International Journal of Computational and Experimental Science and ENgineering (IJCESEN)

Vol. 11-No.1 (2025) pp. 949-953
http://www.ijcesen.com

ISSN: 2149-9144

Research Article

Borrow Save Adder Implementation Under Threshold Voltage Variability

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Article Info:

DOI: 10.22399/ijcesen.1004
Received : 01 November 2024
Accepted : 02 Fenruary 2025

Keywords :

Monte-Carlo simulations,
variation-tolerant design,
timing analysis,
borrow-save,
threshold voltage variation.

Abstract:

It is commonly recognized that lower logic depth enables low voltage operation, which lowers power dissipation. But these circuits are especially prone to fluctuations, which could undermine the anticipated advantages. These short addresses the problem of increased threshold voltage variance by providing a low-power addition method that works under variability. In particular, by quantitatively comparing the effects of variation on the performances of ripple-carry adders (RCA) and borrow-save adders (BSA), the average power reduction that BSA achieves at low voltage values at the expense of increased delay variation is measured. This leads to a suggestion of a method that improves the performance of both adders. The calculated average power dissipation and maximum critical path delay variation of BSA at various supply voltages. It is demonstrated that a significant reduction in supply voltage is achievable, resulting reduction in BSA's overall power dissipation when compared to a counterpart operating at nominal voltage and maintaining a maximum delay lower than that of RCA. Moreover, straightforward design modifications that exchange latency for variability are incorporated in the BSA design, thereby lowering the maximum delay's normalized standard deviation.

1. Introduction

The basic component of all processors' arithmetic units is the adder. In an RCA, the carry output of the preceding full adder is used as the carry input for the subsequent full adder. BSA carries out the carry-free addition algorithm by use of four to two compressors and two complete adders. Compared to an RCA, the borrow save adder has lower latency and power consumption. One kind of digital adder used in computer arithmetic is called a Borrow Save Adder (BSA). Its goals are to lower power usage and boost performance. Now let's review the key points about Borrow Save Adders, especially when threshold voltage variability is present: Though it concentrates on the subtraction operation—where "borrow" is employed in place of "carry"—the BSA is comparable to a Carry Save Adder (CSA).In some instances, quicker arithmetic processes are possible because a BSA performs the subtraction operation without immediately propagating the borrow. The smallest gate-to-source voltage differential required to establish a conducting route between a MOSFET transistor's source and drain is known as the threshold voltage. Temperature variations and other external conditions, as well as manufacturing flaws, can all contribute to threshold voltage variability. Transistor switching speeds might differ depending on variations in the threshold voltage. The overall performance of the adder may be impacted by timing errors caused by this variability, which can lead some transistors to flip quicker or slower than anticipated. Similar to other digital circuits, BSAs may exhibit sensitivity to changes in Vth due to its

impact on the dynamic power consumption and leakage current.

Lower threshold voltages typically result in a trade-off between reduced switching power and increased leakage power. When speed and power efficiency are crucial in high-performance, low-power computing applications, BSAs is the best choice. Section2 describes the existing methods and section3 discusses the proposed method. Section 4 gives results and discussion. Section5 concludes the method.

2. Related works

Due to the significant increase in delay uncertainty in deep sub-micron integrated circuit design, statistical techniques for timing analysis have become essential, rendering conventional approaches for electrical parameter modelling ineffective [1]. The underlying atomic-level unpredictability found in contemporary semiconductor devices, along with the challenges associated with exact process control, explains why produced integrated circuits (ICs) exhibit properties that significantly deviate from their original designs. These challenges, together with the seeming limitations of deterministic static timing analysis tools, push researchers and industry practitioners to search for practical solutions that consider a range of corner cases that characterize delay characteristics in extreme processes and environments. Statistical Timing Analysis shows up as a workable answer in this situation [2,3]. Because of the complexity and increased number of steps in the production process, physical parameters are prone to variation. The parameters are classified into intra- and inter-die variations when statistical modelling is applied. The former, also called die-to-die, is generated by manufacturing process mechanisms or environmental conditions that cause global shifts that are the same across a die, wafer, or lot. The latter, also known as within-die, models device properties with different variations within a die. Although intra-die fluctuations have little effect on parameters in generations of long-channel device manufacturing processes, these variations are taken into account for contemporary digital designs where low supply voltage values are crucial[4]. According to the evaluation, at nominal supply voltage, Less delay variation is achieved using BSA than by RCA. Furthermore, one can achieve the delay constraints imposed by the RCA's delay characteristics by lowering the BSA's supply voltage, which also significantly reduces PDP and power dissipation[5]. The Wallace tree multiplier is implemented by the design and use of several symmetric stacked counters. The suggested multiplier has a PDP of 2.47 and uses 0.798 MW of power. When compared to current techniques, the developed multiplier uses less power while slightly increasing latency[6]. RNS MAC has better delay variation than binary MAC were discussed [7]. Various digital adders are discussed [8]. Performance loss can be caused by process variation, Low energy consumption [9]. This method greatly reduces the power feeding of predicted adders by suggesting certain adjustments. The removal of carry generation from LSB to MSB is one of the conservative building's modifications. This allows the adder to operate at a fast pace while using little power [10,11].

Full-Adder timing margin research is crucial because timing breaches have a detrimental effect on the fundamental functions of all processing systems. We concentrate on the Borrow-Save Adder (BSA) and the Ripple-Carry Adder (RCA), two adder structures with straightforward architectures. The RCA is made up of a bit-length worth of cascading Full Adder (FA) cells. Assuming nominal process and environmental circumstances, its maximum critical route delay is defined by the journey along its carry chain until the sum output of the Most Significant Bit location. The architecture of RCA is shown in figure1. On the other hand, different sensitizable pathways may express the maximum critical path delay when process oscillations occur.

Unlike typical binary arithmetic, BSA uses the radix-2 encoding over the digit set S = {−1, 0, 1}, often known as borrow-save (BS) encoding. We study the latency characteristics of BSA. In BS encoding, each digit (xi) at the ith bit position is represented by a pair of bits (xn, xpi) with positive, negative, and positive weights; so, xi = xp xni∈ S. Adding digits while maintaining the radix-2 BS encoding is made possible by the carry-free addition technique. Three steps are involved in it: Compute the position sums pi = xi + yi; ii) For each pi, there is a transfer (ti+1) and an intermediate sum (wi = pi − r • ti+1), where r is the radix of the representation; and iii. The process involves summing up the incoming transfers to find the total number of digits, which is si = wi + ti [8]. The carry-free addition technique is applied by BSA using two FAs to generate 4-to-2 compressors [12]. Operands already stated in BS encoding are added similarly to operands declared in carry-

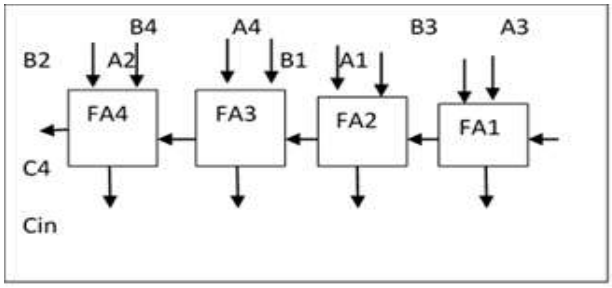

Figure 1. *Architecture of Ripple Carry Adder*

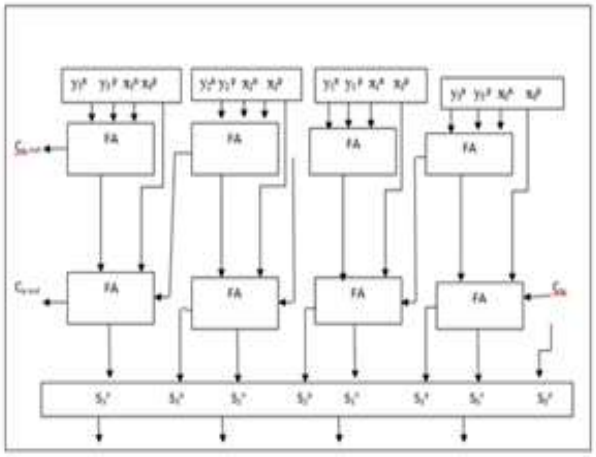

Figure 2. *Architecture of Borrow Save Adder*

save encoding, with a few inversions at the beginning and end of the processing. Figure 2 illustrates BSA architecture's benefit of decreased ripple impact compared to RCA architecture [13,14]. The implementation of BSA, the slow sum-output of the top row FAs drives the input-pin of a bottom row FA that is optimized to receive the slow input. When seven and one with zero carry-in are joined, for example, a carry must be transmitted successively from the first to the fourth bit position along the carry chain in the RCA. Conventional binary encoding for this would be x = 0111 and y = 0001, respectively. The corresponding operation in the BS domain produces the sum s = {(0, 1), (1, 1), (1, 1), (0, 0)}BS, which is calculated with a ti's ripple effect limited to a neighbor bit position. For seven and one, respectively, the corresponding representations are x = {(0, 0), (0, 1), (0, 1), (0, 1)}BS and y = {(0, 0), (0, 0), (0, 0), (0, 1)}BS.

4. Results and Discussion

The Ripple carry adder and Borrow Save Adder are designed using verilog and simulated using Xilinx and cadence software. The Schematic diagram of RCA is shown in figure3

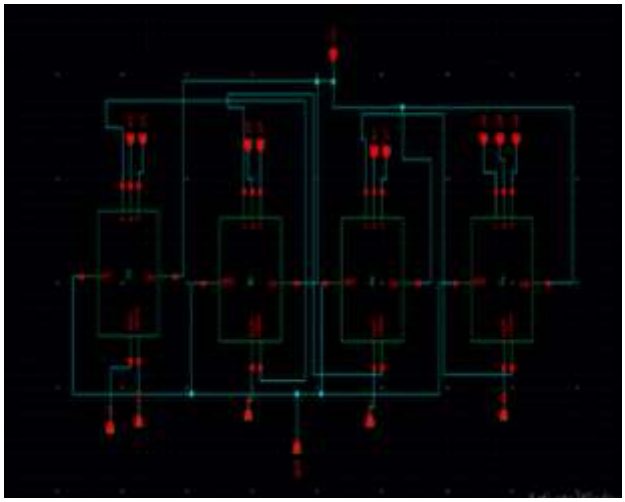

Figure 3. *Shematic design of RCA design*

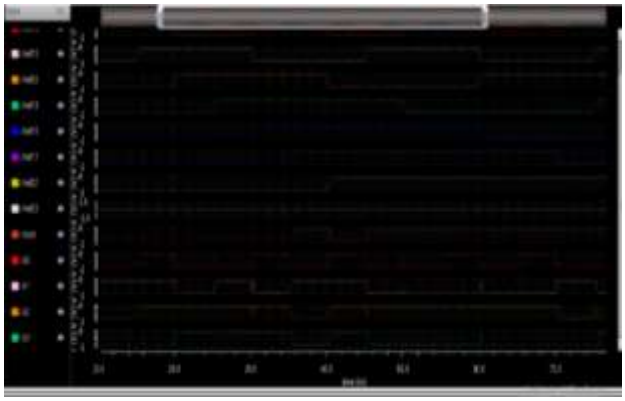

Figure 4. *RCA simulation Output*

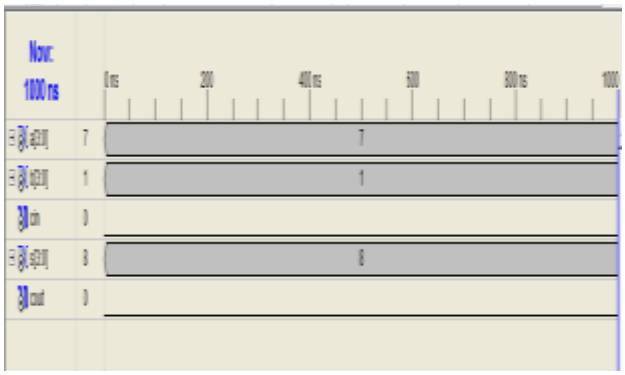

Figure 5. *Simulation output of RCA*

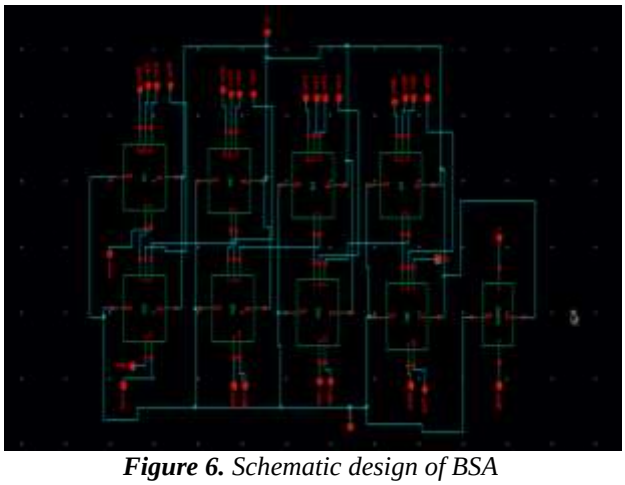

Figure 6. *Schematic design of BSA*

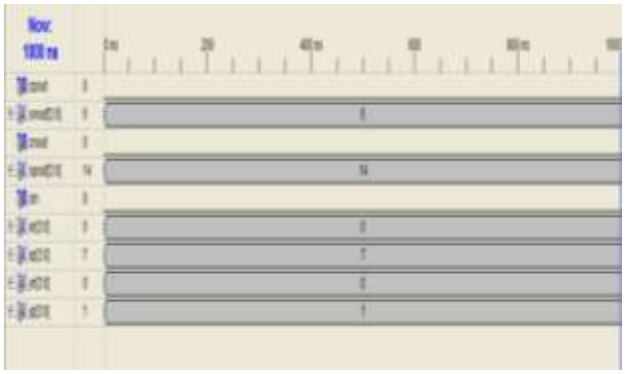

Figure 7. *Simulation output of BSA*

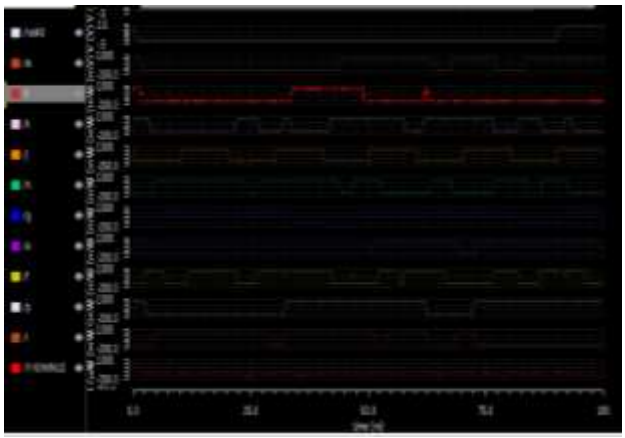

Figure 8. *Simulation output of BSA*

and simulation results are shown in figure 4 and 5. The Schematic diagram of BSA is illustrated in figure 6 and simulation output are given in figure 7 and 8.

The Performance Analysis of power and delay of BSA and RCA for various voltage are given in table 1.

Table 1. *Performance Analysis of BSA and RCA for various voltages*

Voltage(v	BSA		RCA	
	Power(w)	Delay(s)	Power(w)	Delay(s)
5	459.0E-3	45.90E-9	4.131E-3	68.41E-9
3 v	123.6E-3	20.63E-9	4.931E-3	36.76E-9
1.1 v	96.85E-6	-23.7E-9	68.13E-3	44.26E-9
0.9v	68.56E-6	-20.4E-9	56.98E-6	36.36E-9
0.8 v	46.52E-6	-2.71E-9	37.81E-6	9.772E-9

5. Conclusion

With varying supply voltages, the BSA and RCA designs' average power dissipation and maximum critical path delay variation are computed. In comparison to RCA at the same supply voltage, the recommended BSA achieves a lower maximum delay standard deviation. It also demonstrates that supply voltage may be dropped greatly, which reduces the overall power consumption of BSA when compared to a counterpart that maintains a maximum delay below RCA's while operating at nominal voltage. Simple design modifications that substitute variability for latency are also incorporated into the BSA design, which lowers the maximum delay's normalized standard deviation. Monte carlo tools have been applied in different fields and reported [15-18].

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
- **Acknowledgement:** The authors declare that they have nobody or no-company to acknowledge.
- **Author contributions:** The authors declare that they have equal right on this paper.
- **Funding information:** The authors declare that there is no funding to be acknowledged.
- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

References

[1]R. Garg, (2009) Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations. *New York, NY, USA: Springer*.

[2]A. Srivastava, D. Sylvester, and D. Blaauw, (2006). Statistical Analysis and Optimization for VLSI: Timing and Power. *New York, NY, USA: Springer*.

[3] M. Orshansky, S. Nassif, and D. Boning, (2007). Design for Manufacturability and Statistical Design: A Constructive Approach. *New York, NY, USA: Springer*.

[4]M. Eisele, J. Berthold, D. Schmitt-Landsiedel, and R. Mahnkopf, (1997). The impact of intra-die device parameter variations on path delays and on the design for yield of low voltage digital circuits, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 5(4);360–368.

[5]Kleanthis Papachatzopoulos, Vassilis Paliouras (2018). Design and implementation of low power addition of borrow save adder, *IEEE Transaction on circuits and systems-II* 65;572-576.

[6]Kalamani C, Krishnammal V P, Balaji V R, Marimuthu C N, (2024). Energy Efficient Wallace Multiplier Using Symmetric Stacking Counter

Circuit, *Measurement: Sensors*. 35;101267. https://doi.org/10.1016/j.measen.2024.101267

[7]Hamed Dorosti,Ali Teymouri,Sied Mehdi Fakhraie,Mostafa E.Salehi, (2016). Ultra low-energy Variation-Aware Design: Adder Architecture Study, *IEEE Trans.VLSI Syst*, 24(3);1165-1168.

[8]P.Kornerup, (2015). Reviewing high-radix signed-digit adders, *IEEE Trans. Comput*., 64(5);1502-1505.

[9]K.Papachatzopoulos and I.Kouretas, V.Paliouras, (2016). Dynamic delay variation behaviour of RNS multiply-add architecture, in Proc. *IEEE Int. Symp Circuits Syst.(ISCAS)*, pp.1978-1981.

[10]C Kalamani, VK Perumal, MV Kumar, J Muralidharan, (2023). Design of Power and Delay Efficient Fault Tolerant Adder, *Third International Conference on Artificial*.

[11]C. Kalamani., Dharani, Vanjipriya, Ishwarya Niranjana. M, (2023). Design of Power Delay Efficient Wallace Muliplier, *9th International Conference on Advanced Computing and Communication Systems (ICACCS)*.

[12]B. Parhami, (2009). Computer Arithmetic: Algorithms and Hardware Designs. *New York, NY, USA: Oxford Univ. Press*.

[13]C Kalamani, VA Karthick, S Anitha, KK Kumar, (2017). Design and implementation of 4 bit multiplier using fault tolerant hybrid full adder, *Journal of Electronics and Communication Engineering*. *11*, 587-594.

[14]K. Papachatzopoulos and V. Paliouras, (2018). Low-Power Addition With Borrow-Save Adders Under Threshold Voltage Variability, in *IEEE Transactions on Circuits and Systems II: Express Briefs*, 65(5);572-576.

[15]Şen BAYKAL, D., Ghada ALMISNED, Hessa ALKARRANI, & H.O. TEKIN. (2024). Radiation Shielding Characteristics and Transmission Factor values of some Selected Alloys: A Monte Carlo-Based Study. *International Journal of Computational and Experimental Science and Engineering*, 10(4). https://doi.org/10.22399/ijcesen.421

[16]Çağlan, A., & Dirican, B. (2024). Evaluation of Dosimetric and Radiobiological Parameters for Different TPS Dose Calculation Algorithms and Plans for Lung Cancer Radiotherapy. *International Journal of Computational and Experimental Science and Engineering*, 10(2). https://doi.org/10.22399/ijcesen.335

[17]Şen BAYKAL, D. (2024). A novel approach for Technetium-99m radioisotope transportation and storage in lead-free glass containers: A comprehensive assessment through Monte Carlo simulation technique. *International Journal of Computational and Experimental Science and Engineering*, 10(2). https://doi.org/10.22399/ijcesen.304

[18]Şen Baykal, D., ALMISNED , G., ALKARRANI , H., & TEKIN, H. O. (2024). Exploring gamma-ray and neutron attenuation properties of some high-density alloy samples through MCNP Monte Carlo code . *International Journal of Computational and Experimental Science and Engineering*, 10(3). https://doi.org/10.22399/ijcesen.422