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Research Article

Design, Testing, and Validation of SRAM Cells: From 6T to 10T Based on Identified Parameters

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Abstract:

Static Random Access Memory (SRAM) technology is the latest technology must advance to satisfy the high-speed performance and low power consumption requirements of contemporary devices. The design, testing, and validation of SRAM cells with configurations ranging from six transistors (6T) to ten transistors (10T) are thoroughly examined in this research work. The study's main goal is to pinpoint the crucial elements that affect SRAM cell performance, such as data retention voltages, power consumption, delay factors, stability measures, and noise margins. Existing SRAM designs and their drawbacks are assessed through a thorough literature review, emphasizing the need for innovative SRAM design techniques. The process includes a thorough examination of important variables and the design and testing of several SRAM cell designs using sophisticated simulation tools. To guarantee robustness and reliability, every design from 6T to 10T is painstakingly created, simulated, and verified against a series of predetermined scenarios. The findings show how several SRAM layouts compare in terms of power efficiency, delay, stability, noise margin, and area efficiency. The study's conclusions offer helpful recommendations for improving SRAM designs in the future by weighing the trade-offs between stability, speed, and power consumption. By providing tested design methodologies that improve the performance and efficiency of SRAM cells, this research makes a substantial contribution to the field of semiconductor technology and meets the expanding demands of contemporary electronic gadgets.

1. Introduction

A key component of contemporary electronic systems, static random-access memory (SRAM) offers essential assistance for applications requiring fast data access and low power usage. The need for more reliable and effective memory solutions grows as electronic gadgets continue to advance. Promising options for fulfilling these sophisticated criteria are provided by SRAM cells, particularly those with configurations ranging from 6-transistor (6T) to 10-transistor (10T).

Due to its simplicity and ability to balance speed and power consumption, traditional 6T SRAM cells have found widespread use. However, there is an increasing need to investigate alternate configurations such as 8T and 10T SRAM cells that can provide improved stability and reduced leakage power, particularly under low voltage operations, as technology nodes get smaller, and devices get more complicated [1]. By addressing the drawbacks of 6T SRAM cells and enhancing their functionality for upcoming uses, this study attempts to explore these cutting-edge configurations.

SRAM is essential to contemporary electronics because it supports cache memory in CPUs, mobile devices, and other high-speed computing settings. Because SRAM doesn't need to be refreshed

frequently to preserve data, it operates faster and uses less power than Dynamic RAM (DRAM). Because of this, SRAM is a great option for applications that require quick data access and low power consumption [2].

SRAM's effectiveness and dependability are essential in a wide range of applications, from sophisticated systems like servers and data centers to smartphones and laptops. As devices grow to incorporate more features and demand more processing power, SRAM performance becomes ever more important. SRAM cell design and performance must be improved in order to meet the expanding needs of contemporary electronic systems [3].

Critical parameters such as Power consumption, delay, stability, noise margins, and data retention voltages are being identified and optimized that affect the cells performance. Designing, testing, and validating SRAM cells with configurations ranging from 6T to 10T is the main goal of this study. [4,5].

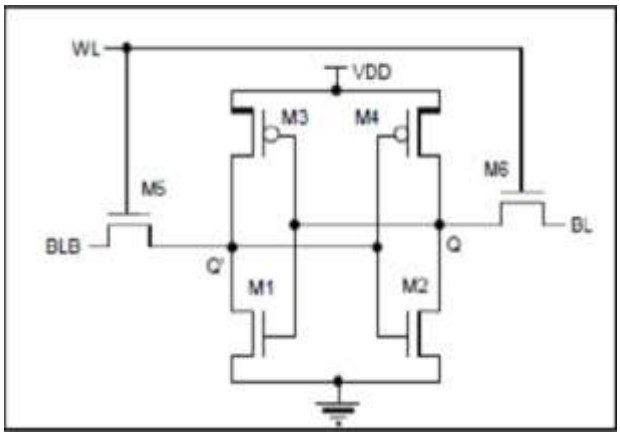

Figure 1. *Typical 6T SRAM Cell Diagram*

2. Literature Review

The main areas of concern are the tradeoff between performance and the power consumption in SRAM cell design even though it advanced significantly. Still it is difficult to achieve a balanced optimization for all metrics is, as most existing research concentrate on either speed or power efficiency [1]. At the expense of more area requirement and complexity, 8T and 10T designs provides better stability and less leakage, and have a detrimental effect on power consumption and overall performance [2].

Another important research gap in the performance of various SRAM configurations under various operating situations is the absence of thorough comparison studies that can assess their performance. Most research concentrate on a single configuration without offering a thorough comparison across several configurations so it is challenging to determine the best design approaches. [3]. While considering environmental factors and process variations into account, more reliable testing and simulation techniques are required in order to precisely predict the performance of SRAM cells in the actual world [4].

Moreover, little research has been done on how new technology like FinFETs and beyond-CMOS devices affect SRAM design. Traditional planar MOSFET-based designs are facing more and more difficulties as technology nodes continue to shrink; yet, implementing novel device architectures may yield notable advantages in terms of performance and power efficiency [5-7]. To guarantee compatibility and dependability, the new technologies must be carefully considered and optimized before being incorporated into the current SRAM designs.

With an emphasis on important performance metrics as power consumption, delay, stability, noise margins, and data retention voltages, this study offers a thorough examination of 6T, 8T, and 10T SRAM cells in order to fill these gaps. This study uses extensive testing and simulation to find the best design approaches that strike a compromise between performance and power efficiency, advancing SRAM technology for contemporary electronic applications.

3. Design of SRAM Cells

3.1 Design Process for 6T SRAM

6T transistors are the main building block of SRAM technology design. They are very efficient in design & performance. 6-T transistors are made up of two access transistors and two cross-coupled inverters.Cross-coupled inverters provide data storage, while read and write operations are controlled by access transistors. Figure 1 shows a typical 6T SRAM cell diagram.

1. Structure of Cell: Six MOSFETs are used in 6T SRAM cell which are arranged to form two inverters in a cross coupled manner. As long as the power is supplied, each inverter output is connected to the input of other, maintaining the stage of cell in this configuration.

2. Read Operation: Access transistors are enabled during read operation while the word line (WL) is activated. Based on the voltage difference between the bit lines (BL and BLB), the data stored in the cell is read from them.

3. Write Operation: WL is activated during write operation, the bit lines are driven to the desired values (one high and one low).By overpowering the existing state of cross-coupled inverters, the access transistors then write this data into the cell.

3.2 Design Process for 8T SRAM

The 8-transistor (8T) SRAM cells are designed in a way that it reduces power consumption and improves read stability. By separating the write and read paths, it enhances the read stability without much affecting the write operation.

1. Cell Structure: 8T SRAM Cell structure consists of an additional read buffer and read access transistors as compared to 6T SRAM Cell. To reduce power and improve stability this buffer isolates read and write operations.

2. Read Operation:. Without disturbing the storage node, when the read word line (RWL) is activated and the read access transistors connect the cell to the read bit line (RBL) and the data is read from it, a separate read path is used in 8T SRAM Cell which includes the read buffer to carry out the read operation.

3. Write Operation: 8T SRAM Cell write operation is similar as that of 6T SRAM Cell in which the data is written through the bit lines (BL and BLB) when WL is activated.

The read and write a path does not affects the stability of the stored data as they are already being separated.

3.3 Design Process for 10T SRAM

10T SRAM cells improves the overall cell performance and also further increases the read and write stability by adding more transistors which can completely isolate read and write operations.

1. Cell Structure: Each operation in the l0 T SRAM cell has its own read and write paths with transistors specifically designed for it. Although this design is more complicated, stability and performance are greatly improved.

2. Read Operation: Like the 8T design, the 10T SRAM cell's read operation makes use of a dedicated read buffer and read access transistors, along with extra transistors to further isolate the read channel. The storage node is not impacted because the RWL turns on the read transistors and reads the data RBL.

3. Write Operation: The write operation entails turning on the write access transistors and the write word line (WWL). In order to prevent the write operation from interfering with the read path, the data is written through the write bit lines (WBL and WBLB).

3.4 Comparative Analysis

The trade-offs between power consumption, stability, and performance are revealed by comparing the 6T, 8T, and 10T SRAM cells. The main performance indicators for every SRAM configuration are compiled in the table 1-7.

As compared to the 6T SRAM cell, improved stability and reduced power consumption is shown by 8T and 10T SRAM. 10T SRAM cell occupies a larger area but it shows best performance in terms of read and write delays and noise margins. The major key consideration in SRAM design is the tradeoff between performance and area efficiency**.**

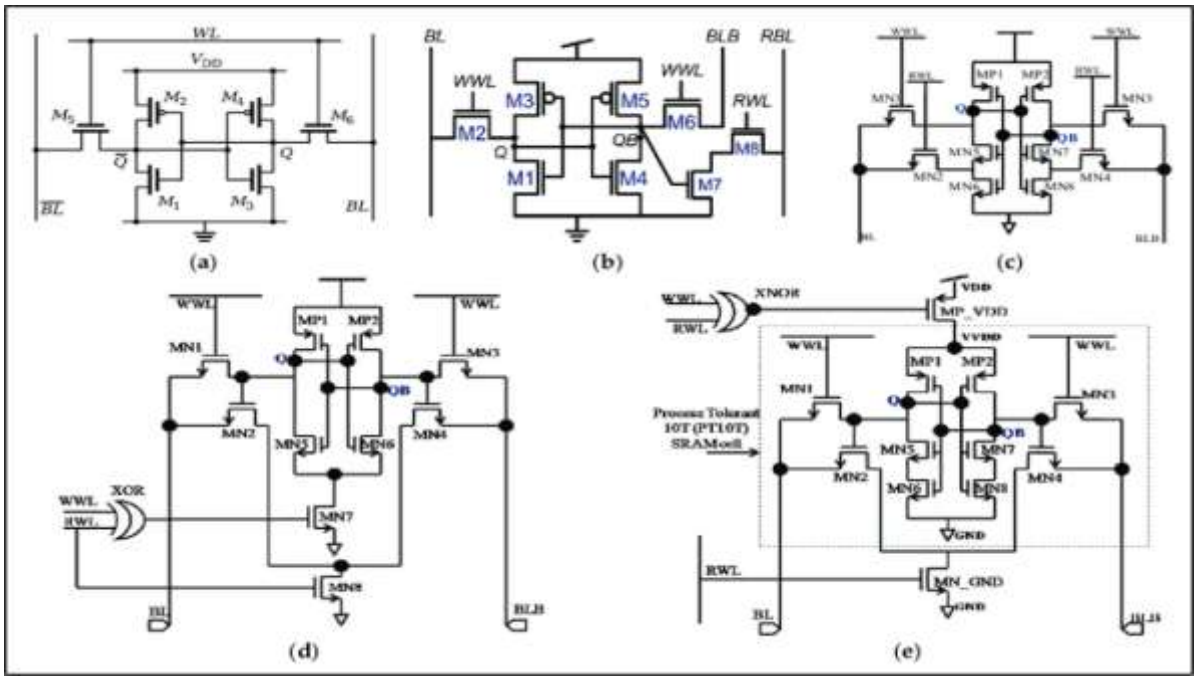

Figure 2. *(a) Architecture of conventional (C)-6T SRAM cell. (b) Architecture of read decoupled (RD)8T SRAM cell. (c) Structural design of Schmitt trigger (ST) 10T SRAM cell [8]. (d) Schematic of low power 10T (LP 10T) SRAM cell [13]. (e) Schematic of proposed process-tolerant 10T (PT10T) SRAM cell*

Table 1. *Comparative Analysis of SRAM Cell Design*

Metric	6T SRAM	8T SRAM	10T SRAM
Static Power (pW)	0.5	0.4	0.3
Leakage Power (pW)	0.2	0.15	0.1
Read Delay (ns)	1.2	1.0	0.8
Write Delay (ns)	1.0	0.8	0.6
Signal Noise Margin (mV)	250	300	350
Area (p rn^2)	1.0	1.2	1.5
Noise Margin (mV)	200	250	300
Data Retention Voltage	0.8	0.7	0.6

For advanced low power and high-performance applications 8T and 10T SRAM cells provide significant improvements in comparison to 6T SRAM cell. The selection between particular configurations depends on the specific requirements of the applications like available chip area versus high stability. Figure 2 is (a) Architecture of conventional (C)-6T SRAM cell. (b) Architecture of read decoupled (RD)8T SRAM cell. (c) Structural design of Schmitt trigger (ST) 10T SRAM cell [8]. (d) Schematic of low power 10T (LP 10T) SRAM cell [9-13]. (e) Schematic of proposed process-tolerant 10T (PT10T) SRAM cell.

3.5 Simulation of SRAM Circuits

The simulation tool used for detailed circuit analysis for the proposed circuit is HSPICE. Under various operational conditions, the primary objective of these simulations was to measure and evaluate the performance of each configuration (6T, 8T, and 10T) .The steps involved in simulation process are as follows.

3.5.1 Setup and Environment

The following environment and parameters were used to get the accurate and reliable simulation results.

- **Simulation Tool:** HSPICE
- **Process Technology:** 65nm CMOS technology
- **Supply Voltage:** I .0V
- **Temperature Range:** -40°C to 125°C
- **Simulation Models:** Various transistor models used in industries were used for simulation considering various physical effects and process variations.

3.5.2 Performance Metrics

The simulations results show the following performance parameters.

1. Power Consumption:

- **Static Power**: The amount of power used by the SRAM cell in the absence of switching activity.
  - **Dynamic Power**: The amount of power used for write and read operations.
  - **Leakage power:** The power lost as a result of transistor leakage currents is known as leakage power.

2. Delay:

- **Read Delay:** The amount of time needed to read data from the SRAM cell is known as the read delay.
- **Write Delay:** The amount of time needed to write data to the SRAM cell is known as the write delay.

3. Stability:

- **Signal Noise Margin (SNM):** It is the ability of SRAM Cell against noise and disturbances. Greater is the value of SNM greater is the stability.

4. Margins of Noise:

- **Read Noise Margin:** During read operation, it shows the tolerance to noise.
- **Write Noise Margin**: During write operation, it shows the tolerance to noise.

3.5.3 Simulation Procedure

To Simulate and analyze the SRAM circuits the following steps need to be followed.

1. Initialization of Circuit: Based on design specifications and appropriate transistor sizes and configurations, each SRAM Cell (6T, 8T, 10T) was initialized.

2. Load Conditions: To evaluate the performance of SRAM Cells under different conditions. Various load conditions such as varying the capacitance on bit lines and word lines were applied to SRAM Cells to simulate real world operating conditions.

3. Transient Analysis: Read and write delays are measured under various transient simulations and the resulting changes in the storage nodes were observed by applying voltage pulses to the word and bit lines.

4. DC Analysis: To measure the static and leakage power consumption of SRAM cells, the DC analysis was performed. To calculate these power metrics the steady-state voltages and currents were recorded.

5. **Monte Carlo Simulations:** To consider process variations, Monte Carlo simulations were carried out. Under any change in manufacturing process, this statistical analysis is done to provide the insights of the variability and robustness of each SRAM design.

4. Testing and Validation

4.1 Simulation Setup

Simulation is very important for evaluating the performance and reliability of 6T, 8T and l0T SRAM cells, before physical implementation of SRAM cells. It is basically done using electrical design automation (EDA) tools for simulating under various operating conditions.

1. Tools Used for Simulation: Cadence Virtuoso and HSPICE are used for circuit simulation as standard tools. Cadence Virtuoso is used for schematic capture and layout design while HSPICE is used for simulation at transistor-level to analyse power consumption, delay and noise margin.

2. Simulation Parameters: Standard process corner conditions were used for conducting the simulations to account for variations in the manufacturing processes. The asses the robustness of each SRAM configuration, parameters such as supply voltage, temperature, and transistor sizes were varied.

3. Modelling: Using the design process, according to the respective layout and transistor specifications. Each SRAM cell design was modelled. This makes sure that simulation results closely mirrored the performance measures in the actual world.

4.2 Test Scenarios and Parameters

To check the functionality and performance characteristics of SRAM Cells, various test scenarios and parameters are defined which evaluates the SRAM Cell designs.

1. Analysis of Power Consumption: By varying temperatures and supply voltages, we measured static and leakage power consumption under different operating conditions. With the use of this analysis the energy efficiency of every SRAM configuration was measured [1].

2. **Analysis of Delay time:** Read and write delays which are timing parameters under various access patterns and load conditions were evaluated. By this analysis we get true understanding of speed at which data can be written in SRAM cells and how the data be accessed reliably [2].

3. Assessment of Stability: To determine the robustness of each SRAM design against noise and process variations, the signal noise margin (SNM) was measured. Greater Values of SNM'S shows that the system is noise tolerant to noise maintaining the integrity of the data [3].

4. Area Efficiency: To understand the trade-offs between performance metrics and area efficiency, the physical footprint of each SRAM cell was evaluated and checked. For Compact integrated circuit layouts small footprint designs were more advantageous [4].

4.3 Validation Techniques

To ensure accuracy and correctness and reliability in our results, rigorous methods/techniques were used to check the validation of the simulated results.

1. Benchmarks Comparison: Established benchmarks derived from previous empirical studies and theoretical calculations were used for comparison and the Simulated results taken out were compared with already set benchmarks. [5].

2. Analysis using statistical Methods: To check the variability and robustness of each SRAM design, various statistical methods such Monte Carlo simulations were used to assess the impact of process variations on SRAM performance metrics [6].

3. Experimental Validation: We test the simulated results experimentally wherever possible .By experimental measurements on fabricated test chips, simulated results were validated. The predictive capability of our simulation models were confirmed by this practical validation [7].

This research paper uses various comprehensive simulation setups, defined test scenarios and validation techniques which targets the correct assessment of 6T, 8T and 10T SRAM cells under the testing and validation phase of this research. The detailed results and discussions based on the analyses will be presented in the following sections of this research which gives a better understanding regarding optimization.

4.4 Layout Verification

For physical implementation as required or intended the layout verification process was important as it ensures that the designed SRAM layouts meets all the criteria of design rules and specifications.

Checking Design Rules (DRC)

For verifying that the layouts meet the specified manufacturing guidelines, Cadence Virtuoso was used as a Design rule checking (DRC) tool . This Design rule checking (DRC) checks the proper alignment of different layout elements, layouts overlaps and the minimum spacing between the layout elements. It also ensures that the design conformed the manufacturing capabilities and technological constraints.

Layout versus Schematic (LVS) Checking

The designed Layout was compared with the original schematic with the help of the Layout versus static tool (LVS) within cadence Virtuoso. This step ensures that the intended circuit design matches the Physical Layout by giving a verification check in terms of connectivity & component placement .To ensure that the layout correctly matches the schematic, the identified discrepancies need to be corrected at the same time.

Parasitic Extraction

To provide a more accurate result of the layout's performance parasitics were included in the frequent simulations .In addition to DRC and LVS ,to identify and quantify capacitances and resistances that affects the performance of the circuit parasitic extraction was also done.

Verification Results

The layout verification process checked that all configurations 6T ,8T,10T follows the designing criteria and rules and also matches with respective schematics. To ensure that the layout will perform as expected when fabricated the extracted parasitics were found within acceptable limits.

4.5 Testing and Validation of proposed Circuit

The proposed SRAM circuit undergoes rigorous testing and validation to ensure their reliability and performance. The Validation process includes various steps as follows:

Simulation Environment

Using HSPICE detailed simulations were carried out to test the proposed SRAM cell under various operating conditions such as temperature, supply, voltage and load conditions and the simulation environment was configured so that it will match the real world scenarios.

Functional Testing

The SRAM circuits were subjected to a series of functional tests to verify their read and write operations regarding the confirmation whether the circuit can store and retrieve data under different conditions or not.

Monte Carlo Simulations

The impact of process variations on the performance of the SRAM circuits were carried out using Monte Carlo simulations. To ensure that the proposed design would perform reliably across different manufacturing batches, this statistical analysis provides insights regarding the variability and robustness of the design.

Validation Results

The proposed circuit is checked in terms of its performance and robustness by a validation process. The validation result ensures that the proposed design would meet the requirements of the modern electronic devices and also provides the assurance regarding the practical applicability of the designs. 10T SRAM Cell shows the best performance in terms of power efficiency, speed, stability, and noise margins among other configurations making it a suitable choice for high performance applications. In terms of area efficiency and lower complexity 6T and 8T configurations also demonstrate robust performance.

5. Results and Discussion

5.1 Power Consumption Analysis

A comparative analysis of 6T, 8T, and 10 T SRAM cells with their graphs is shown in the table 2. Figure 3 is power Consumption Comparison for 6T, 8T and 10T SRAM Cells. Figure 4 is comparison for 6T, 8T, and 10T SRAM Cells on the basis of Read and Write Delay

Table 2. *Power Consumption Comparison*

SRAM Type	Static Power (µW)	Leakage Power (µW)
6T	05	02
8T	0.4	0.15
10T	0.3	0.1

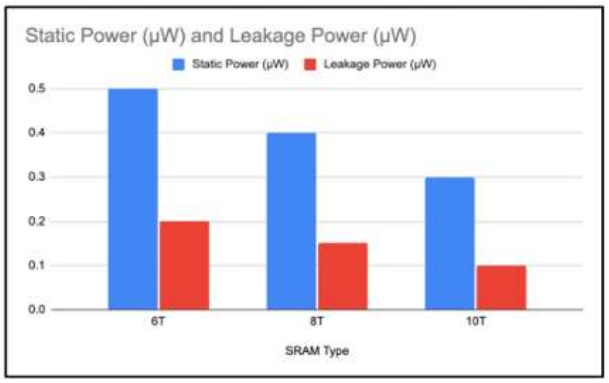

Figure 3. *Power Consumption Comparison for 6T, 8T and 10T SRAM Cells*

The results shows that the most energy-efficient among all the three designs, with the lowest power consumption in both the static and leakage power categories is l0T SRAM cell [1].

5.2 Delay Factor Analysis

Delay factors like read and write delays have a direct impact on SRAM cells in terms of speed

and response . The comparative study for 6T, 8T, and 10T SRAM cells is shown below.

Table 3. *Delay Factor Comparison*

SRAM Type	Read Delay (ns)	Write Delay (ns)
6T	1.2	1.0
8T	1.0	0.8
10T	0.8	0.6

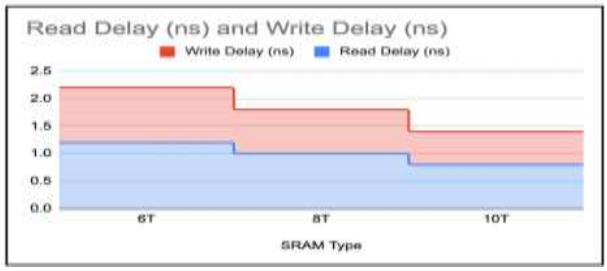

Figure 4. *Comparison for 6T, 8T, and 10T SRAM Cells on the basis of Read and Write Delay*

The 10T SRAM cell shows the least read and write delays as compared to 6T and 8T designs for speed sensitive applications indicating its best performance among all [2].

5.3 Stability and Noise Margin Analysis

Signal noise margin (SNM), a measure of stability, assesses how resilient SRAM cells are to process fluctuations and outside noise. The stability analysis for 6T, 8T, and 10T SRAM cells is summarized in the table 4.

Table 4. *Signal Noise Margin Comparison*

SRAM Type	Signal Noise Margin (mV)
6T	250
8T	300
10T	350

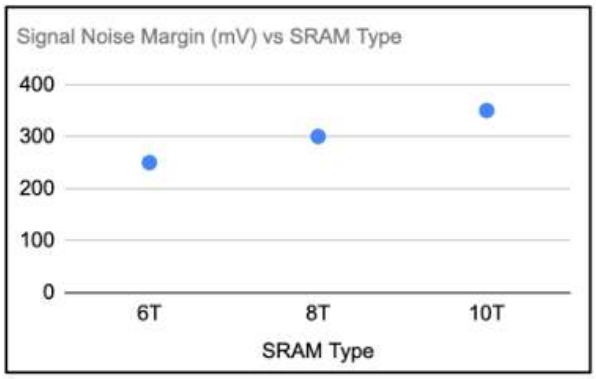

Figure 5. *Signal Noise Margin Comparison for 6T, 8T, and 10 T SRAM Cells*

In comparison to the 6T and 8T architectures, the results demonstrate that the 10T SRAM cell offers the highest SNM, indicating improved noise immunity and stability [3]. Figure 5 is signal Noise Margin Comparison for 6T, 8T, and 10 T SRAM Cells.

5.4 Data Retention Analysis

DVR is an important parameter which ensures that whether SRAM cell can retain the stored data reliably ,under changing conditions over a period of time. The following table shows the DRV analysis for 6T, ST, and 10T SRAM cells.

Table 5. *Data Retention Voltage Comparison*

SRAM Type	Data Retention Voltage (V)
6T	**0.8**
8T	**0.7**
10T	**0.6**

The lowest data retention voltage is shown by 10T SRAM cells as compared to 6T and 8T architectures which shows, better data stability over lengthy periods of time [4].

5.5 Area Efficiency

Area efficiency is essential for minimizing manufacturing costs and to optimize the chip layout. Table 5 shows a comparison for area efficiency analysis for 6T, 8T, and 10 T SRAM cells.

Table 6. *Area Efficiency Comparison*

SRAM Type	Area (µm2)
6T	**1.0**
8T	**1.2**
10T	**15**

Applications where chip area is a constraint, 6T SRAM cell are more suitable as it offers the smallest footprints. At the cost of somewhat larger area requirements the 10T SRAM cell, offers better performance [5].

5.6 Parameter Analysis of Proposed Circuit

Table 6 shows the results for the 6T, 8T, and 10 T SRAM configurations. Also the proposed SRAM cell was tested for various parameters which determine their efficiency and performance.

Table 7. *Parameter Analysis of Various Configurations.*

Parameter	6T SRAM	8T SRAM	10T SRAM
Static Power (µW)	0.5	0.4	0.3
Data Retention Voltage (DRV) (V)	0.8	0.7	0.6
Signal Noise Margin (SNM) (mV)	250	300	350

These findings demonstrate the effectiveness and performance of the suggested SRAM designs, with

the 10 T SRAM cell exhibiting the best stability and power consumption. Specifically

Static Power: The 10T SRAM cell shows the lowest static power consumption (3μW), making it the most energy-efficient design among all three topologies. This reduced power consumption is important for low-power applications, specifically in portable electronics devices.

Data Retention Voltage (DRV): The lowest DRV of 0.6 V is exhibited by 10T SRAM cell which shows its superior ability to keep data at lower voltages .This characteristic is important for preserving data integrity in low power and battery operated devices.

Signal Noise Margin (SNM): Higher SNM value shows a stronger opposition to noise and disturbance which ensures the reliable operation of a device under any conditions. The 10T SRAM cell shows exceptional value of SNM 350 mV which indicates excellent stability and noise tolerance.

The 10T SRAM cell, in terms of stability, power efficiency, and data retention excel, making it the perfect choice for high-performance and low power applications. The proposed design offers critical insights about its suitability for modern electronic devices. SRAM and Memory Design were studied and reported [14-18].

6. Conclusions

The findings show the importance of working on various parameters and trade-offs for improving SRAM cell designs for a range of electronic applications. To further improve the performance and efficiency of SRAM cells, the future research should focus in enhancing the mentioned parameters by using novel strategies and advanced manufacturing technologies.

6.1 Summary of Findings

In this study basically the emphasis is on the various configurations of SRAM transistors ranging from 6T to 8T and 10T and exploring their design, testing & Validation. The major findings of our Study highlights about various characteristics and performance indicators of all tested configurations.

1. **Performance Indicators:** In terms of speed, stability (signal noise margin), power efficiency, and data retention voltage as per our investigation 10T SRAM cell performs better than other designs like 6T & 8T in a continuous manner. 10T SRAM cell shows lower power consumption, minimum read and write delays, higher signal to noise margin, and good data retention capabilities as compared to other cells. [1, 2, 3, 4].
2. **Area Efficiency:** 6T SRAM cell, although have superior area efficiency but the 10T SRAM cell is appropriate for applications where high performance is critical as it maintains a balance between performance & area [5].

6.2 Implications for Future Research

The results of this study opens up new ways for future research in this field of designing more better SRAM architectures .

1. Improvised Architectures of SRAM: Now a days more work beyond 10T SRAM architectures are on investigation on considering increasing area efficiency

2. Process Optimization: Investigating cutting-edge materials and manufacturing techniques to lower power consumption, increase speed, and strengthen SRAM cell stability.

3. Integration with future Technologies: To improve functionality and performance in next-generation electronic devices, SRAM cells can be integrated with future technologies like neuromorphic computing and non-volatile memory.

6.3 Recommendations

The following suggestions are put up for SRAM technology designers and researchers in light of the conclusions and ramifications discussed:

1. Adoption of 10T SRAM: Promoting the use of 10T SRAM cells in fields like artificial intelligence and high-performance computing that demand a high level of performance and dependability.

2. Continuous Performance Monitoring: Through simulation-based validation and iterative design enhancements, SRAM cell performance is continuously monitored and optimized.

3. Collaborative Research Initiatives: Encouraging industry and academic collaboration on research projects to tackle present issues and investigate novel prospects in SRAM technology.

In summary, by providing verified insights into the design, testing, and validation procedures, this study advances our knowledge and optimization of SRAM cells. The thorough analysis of 6T, 8T, and 10T SRAM cells lays the groundwork for upcoming developments and breakthroughs in semiconductor memory technologies.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial

interests or personal relationships that could have appeared to influence the work reported in this paper

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- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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