International Journal of Computational and ExperimentalScience and Engineering (IJCESEN)
Vol. 1-No.2 (2015)pp. 1-6
http://dergipark.ulakbim.gov.tr/ijcesen

***ISSN:*2149-9144**

Modeling and simulation of 8-bit Current-Mode Successive Approximation Registers ADC by using Simulink

Toufik SMAIL[1]*, Salah HANFOUG[2] and Hocine BELMILI [1]

[1]U.D.E.S Solar Equipments Development Unit, BP386, Bou-Ismail, 42415, Wilaya of Tipaza, Algeria, EPST/CDER
[2]Advanced Electronics Laboratory (LEA), University of Batna, Avenue ChahidBoukhlouf, 05000, Batna, Algeria.

* Smail toufik.77@gmail.com

Presented in "2nd International Conference on Computational and Experimental Science and Engineering (ICCESEN-2015)"

Keywords
Analog to Digital Converter
current-mode.
current steering DAC
successive approximation ADC

Abstract: Nowadays the modeling is very important step in the integrated circuits design. For complex circuit architecture such as the Data Converter, in this paper, we developed new ideal model of 8-bit current-mode successive approximation analogue to digital converter (SAR-ADC). The proposed model is implemented in Matlab Simulink environment; the system is modeled by constructing a set of subsystems in SIMULINK environment with different blocks, non-ideal effects are not yet implemented, the main blocks of current-mode SAR ADC are a current sample and hold, a current comparator, SAR logic register and current steering digital to analogue converter (DAC). The simulation results with the static and dynamic performance, confirm the good performance and the high accuracy of the model.

1. Introduction

Due to the huge increase of the architecture and the complexity of mixed signal circuits, the use of behavioral model is necessary to design and simulate the performance of those circuits [1-2-3-4-5], Nowadays the modeling is very important step in the integrated circuits design. For complex circuit architecture such as the Data Converter, the modeling output helps the designer by confirming the performance characteristics of circuits and checking their electrical specifications; Modeling and simulation have increased the designer efficiency and ability to develop increasingly complex and useful electronic circuits, particularly at the integrated circuit (IC) level. Each type of circuit considered has its own particular requirements, in terms of design performance (specifications), design methodologies required to realize the design, modeling and simulation toolsets utilized, designer experience and skills set. Research in analog integrated circuits has recently gone in the direction of low-voltage (LV) , low-power (LP) design, especially in the environment of portable systems where a low supply voltage generated by a single-cell battery is used. These LV circuits have to show also a reduced power consumption to maintain a longer battery lifetime. In this area, traditional voltage mode techniques are going to be substituted by the current-mode approach. Selecting architecture is important since each analog-to-digital converter (ADC) architecture has specific advantages with respect to sampling rate, noise, resolution, dynamic range, power consumption, and implementation area [6]. The Successive approximation ADC (SAR ADC) has been known as a suitable low-power solution for many years [5]. The design of high-performance ADCs

presents difficult challenges as applications call for higher speed and resolutions, and as device dimensions and supply voltages are scaled down [7]. For this purpose the current-mode technique brought many solutions for compatibility with low power supply, high speed and small chip area. The SAR ADCs have received renewed attention due to their excellent power efficiency and low-voltage potential compared to pipelined and cyclic ADCs [6]. Since it does not require operational amplifiers, the voltage mode SAR ADC uses only a comparator and capacitors array in DAC circuit part. This raises two main issues; the first one is the need for large chip area and the second issue is the long settling time [5]. in the other part the Power consumption in the voltage SAR ADC is mainly from the DAC [8], For this reason, the current mode SAR ADC is designed with current source array serving in the DAC for decreasing the effect of long settling time and the power consumption. Moreover, No capacitors are used in the DAC and thus can be made very small compared to voltage SAR ADC [9].

In this paper, a new ideal model of the current-mode SAR ADC is introduced to predict the static and dynamic performance of this type of circuit. The main advantage of this behavioral modeling approach is that offer a low computing time and it is characterized by a less complexity of design in comparing to level transistor method. The proposed model is implemented in the popular Matlab Simulink environment, non-ideal effects are not yet implemented and only basic functionality is checked, These model are implemented by using elementary Simulink of library blocks with take in consideration the computational cost is minimum as possible. The current mode SAR ADC consists of current-mode block such as current Sample and Hold, a current comparator, a current steering DAC and SAR logic register [5].

This paper is organized as the flowing; after the introduction, the behavioral model of SAR ADC is presented in the second section. The different parts of the model are reported in the third section of the paper. Finally, Simulation results and conclusion can be found in the fourth and the fifth sections respectively.

2. The ADC architecture

The block diagram of current mode SAR ADC architecture is shown in Fig. 1. The current steering DAC is the critical building block of the current mode SAR ADC. The operation principle of this current mode SAR ADC is similar to the conventional voltage mode SAR ADC [5]. However, current-mode converters are now demonstrating excellent characteristics and in particular, high resources efficiency (power and area) [10]. The ADC works by using a DAC and comparator to perform a binary search to find the input voltage. A sample and hold circuit (S&H) is used to sample the analog input and hold the sampled value whilst the binary search is performed. The binary search starts with the Most Significant Bit (MSB) and works towards the Least Significant Bit (LSB). For a 8-bit output resolution [11], and in contrast to voltage mode, the current mode ADC uses only CMOS transistor in the DAC as current sources and logical operation. This has the advantage to reduce the area requirements, reduce power consumption and achieve high speed operation [10].

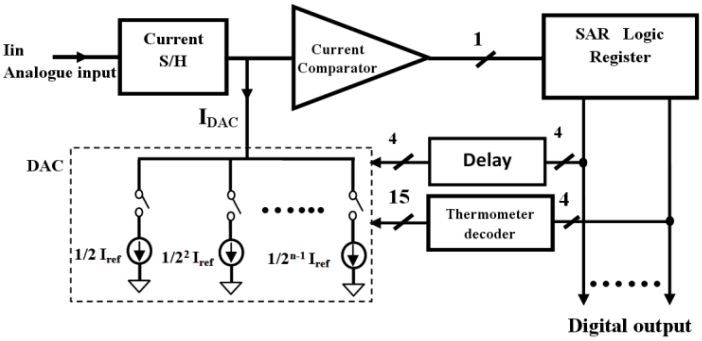

Figure1. *Current mode SAR ADC architecture*

3. Simulink behavioral model of SAR ADC

Simulink model of current mode SAR ADC is shown in Fig 2. It consists of five major blocks; a current S&H, a current comparator, a SAR logic register, a thermometer decoder, and 8-bit current steering DAC with 4 MSB and 4 LSB

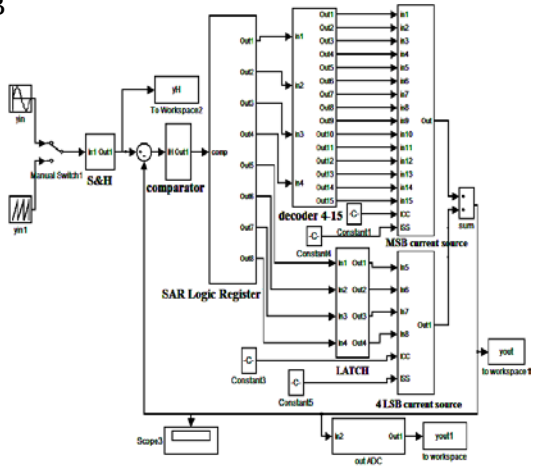

Figure2*.Simulink model ideal of current mode SAR ADC*

As shown in Fig. 3, the basic functionality of a current-mode SAR ADC is similar to voltage mode SAR ADC. The analog input current Iin is sampled by the S&H, the current comparator generate binary bits by the comparing the values of the S&H with the output of the current DAC. To implement the binary search algorithm, the N-bit register is first set to midscale, this is done by setting the MSB to '1' and all other bits to '0'. This forces the DAC output current IDAC to be half of the reference current IREF (IDAC = IREF/2). The S&H current I S/H is then compared with the IDAC. If IS/H is greater than IDAC, the comparator output is logic 1 and the MSB of the N-bit register remains at 1. Conversely, if IS/H is less than IDAC the comparator output is logic 0 and the MSB of the register is changed to 0. Then, the SAR control logic moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is completed, and the N-bit digital word is available in the register.

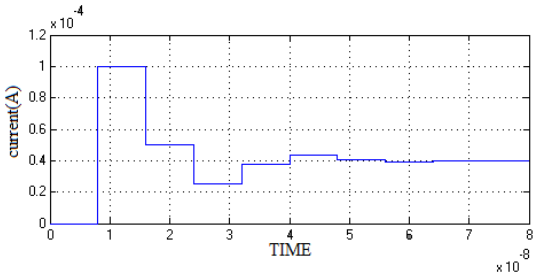

***Figure3**. 8-bit Current mode SAR ADC operation*

3.1. Sample and hold model

ADCs employ a S&H circuit in front end to achieve high precision, linearity and dynamic range [11].The S&H samples the analogue input signal and holds the value for certain time, the model ideal of the sample and hold is shown in Fig. 4.

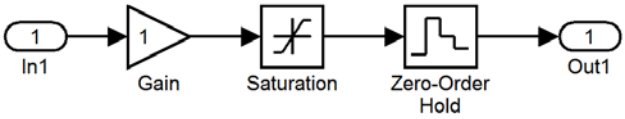

***Figure4**. Sample and Hold model*

3.2. Comparator model

The comparator is a key component of the data converter as it is the link between the analogue and digital domain [12]. In the comparator model as shown in Fig. 5, the input is the subtraction between the output of the S&H and the DAC. On the top of this, a constant value is added to this subtraction to model the offset of the real comparator (in the ideal case the value of the offset is zero). The result is then multiplied by a gain that represents the amplification stage. Then the result is saturated to full logic levels and compared to zero to define which of the two inputs the highest one is.

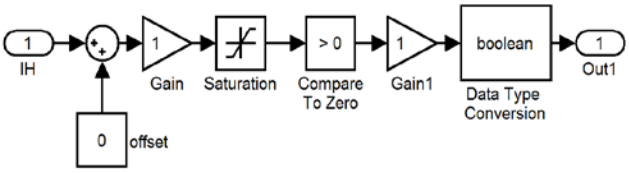

***Figure5**. Comparator model*

3.3. SAR Logic Register

The SAR logic Register is the heart of the system. It generates the controls signal used by the current steering DAC. The logic block (as shown in Fig. 6) has been implemented using two shift registers in order to perform the successive approximation routine. Each shift register is composed of a chain of nine D Flip-Flops. The shift register on the top is used as a sequencer and is synchronous with the internal clock. The bottom register stores the conversion value. Each sampled value (sampling is performed by S&H) of the analogue signal current input is compared by the current comparator with the output of the current DAC. The result of the comparison is used then by the SAR to elaborate the next step.

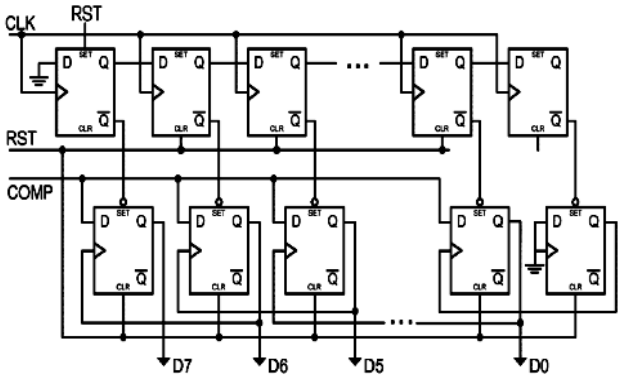

***Figure6**. SAR logic register.*

4-bit binary inputs are converted to 15-bit thermometer codes by the mean of a 4-to-15 binary-to-thermometer decoder, this decoder is constructed by using OR and

AND gates available in SIMULINK library. The decoder is shown in Fig. 7

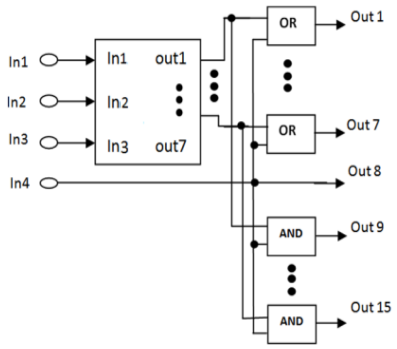

Figure7. *4 to 15 binary thermometer decoder*

3.4. The current steering DAC

The current steering DAC is suitable for high speed and high resolution application [13]. Fig. 8 shows the overall structure of the 8-bit current-steering DAC. The 8-bit input binary data is segmented into the 4 most significant bits (MSBs) and 4 least significant (LSBs), for 4 MSBs bits are decoded by the thermometer in order to control 15 identical current sources, such as the first MSB bit control 23 current source, the second MSB bit control 22 current sources, the third MSB bit control 21 current sources, and the fourth MSB bit control 20 current sources, and 4 least significant (LSBs) are directly applied to the 4 current sources.

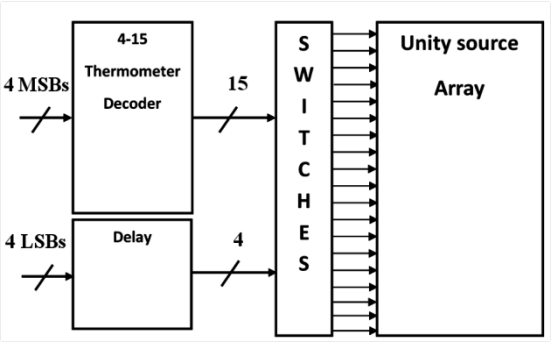

Figure8*. General structure of the 8-bit current-steering DAC*

In the DAC model, each current source is multiplied by gain factor in such a way it became equal to the current source value, the model of switches and current sources array controlled from 4 MSBs, the model of DAC for 4 LSB it is shown in Fig 9.

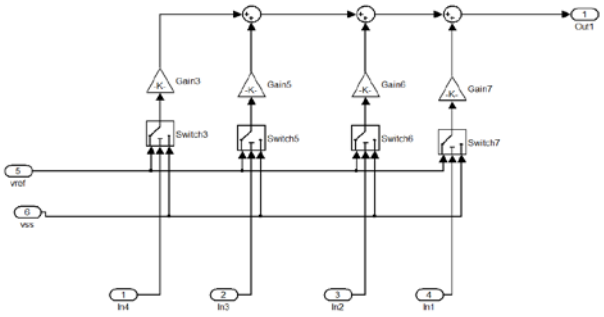

Figure9. *Model of switches and current sources.*

4. Simulation results

To check and to confirm the performance of the new proposed model, simulation is performed and its results are reported in this section with the static and the dynamic performances.

4.1. Dynamic performance

In order to test the ideal model and to confirm its dynamic performance, an analogue signal equivalent to a sine wave with a frequency of 63 KHz is applied to the input of the ADC with sampling rate of 5 MHz as shown in Figure 10. Simulation results of the output signal from the DAC and reconstructed analog signal from ADC are shown in Fig 11 and 12.

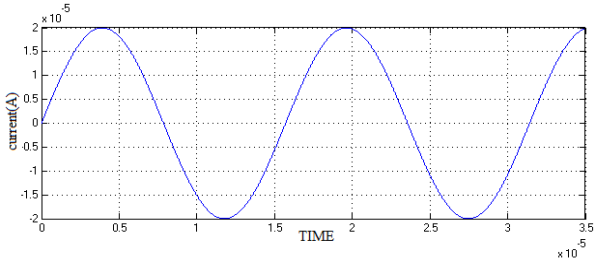

Figure10*. The analogue input signal*

The dynamic performance including Signal to Noise Ratio (SNR), Spurious-Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD). By using the Fast Fourier

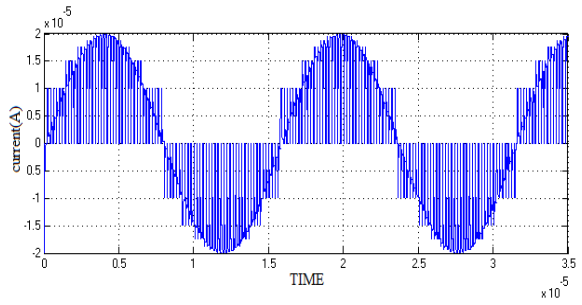

***Figure11**. The analogue signal output from the DAC*

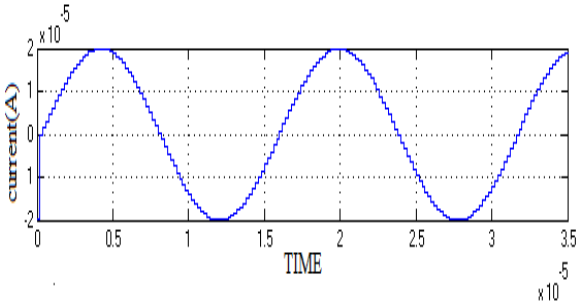

***Figure12**. The analogue signal reconstructed from the output of the ADC*

Transform (FFT), the SFDR and THD can be calculated from the power spectrum. The FFT of the output signal for an ideal model of current mode SAR ADC is shown in Fig13. For the ideal model we extracted a SNR is 49.92dB, The SFDR is 66 dB and the effective number of bits is ENOB=7.9dB.

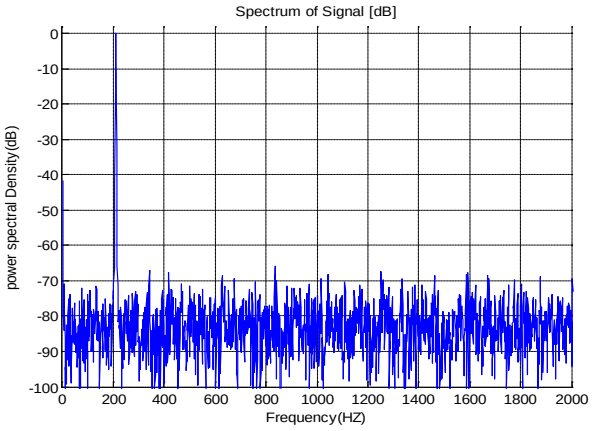

***Figure13**. FFT of the ADC output signal in the ideal case with Fin = 63 kHz; Fs = 12.5MHz*

4.2. Static performance

The linearity is the most important parameter in the data converter. The linearity performance includes Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). The INL is defined as the maximum deviation of a transition point of a conversion from corresponding transition point of an ideal conversion. The INL is simulated using a MATLAB code. Based on INL definition, the LSB will be the deviation of the real transfer function from a straight line. For the DNL, it is defined as the difference between an actual step width and the ideal value of 1LSB. Hence, INL will represent cumulative DNL errors. The DNL is simulated using MATLAB code based by this equation:

$$INL_J = \sum_{i=1}^{j-1} DNL_J$$

The simulation results of DNL and INL are shown in Fig 14 and 15 respectively. The results are of a 8-bit current mode SAR ADC for ideal model. The simulation results show that the variation of the DNL and INL is more or less around 1LSB, it is between +0.14/-0.13 LSB for DNL, and for INL it is in the range of INLmax of +0.35 LSB and INLmin of -0.35 LSB.

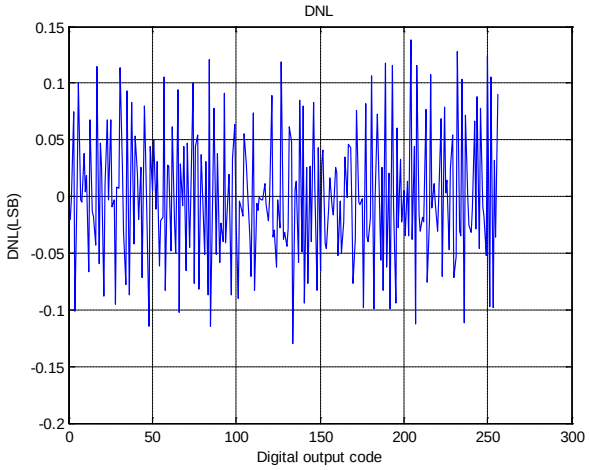

***Figure14** DNL of the ideal 8 bit current mode SAR ADC*

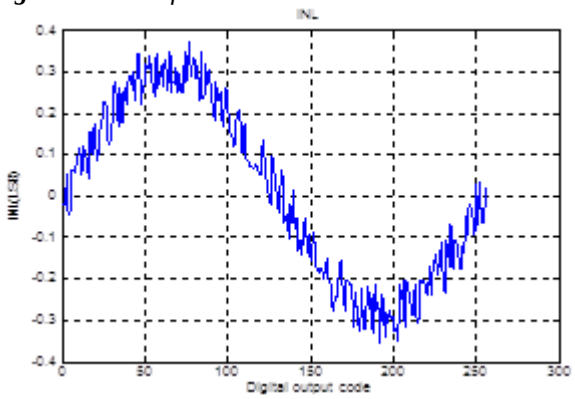

***Figure15**. INL of the ideal 8 bit current mode SAR ADC*

From the results presented in the previous section we can comparison between our behavioral ideal ADC model, and real ADCs with current and analogue mode [5-14-15] can be seen in Table 1. There is a good match between the proposed models and the real ADCs with

current and voltage mode, this proves the accuracy of our behavior model.

Table 1 Comparison the Performance of the current mode SAR ADC MODEL.

Parameters	This work/ Ideal model	[5]	[14]	[15]
VDD	1V	1.2v	1.4v	1.8v
Mode	I-Mode	I-Mode	voltage mode	voltage mode
Resolution (bit)	8	8	8	10
INL (LSB)	-0.35/0.35	-0,56/0:9	-0.2/0.27	-1.02/0.824
DNL (LSB)	-0.13/0.14	-0,84/1:0	-0.18/0.34	-0.2/0.6
SNR (dB)	49.25	/	/	/
SFDR (dB)	65.3	61.64	/	72.025
SNDR (dB)	49.2	46.2	48.2	60.55
ENOB (bit)	7.9	7.38	7.8	9.767

5. Conclusions

A new model of ideal 8-bit current mode SAR ADC has been reported. The analogue blocks are modeled in ideal case. For current comparator, it has been modeled by taking into account that the offset and the delay time of the comparator are equal to zero. For sample and hold, the effect of the charge injection, clock feedthrough, clock jitter and the switching noise have been neglected in this work. The analysis of static and dynamic performances using MATLAB environment confirm the good performance of the model. The behavioral model and the simulation results will help the designer to achieve 8-bit current mode SAR ADC circuit with a low power, a current range in the scale of µA and high efficiency in the chip area by using steering current DAC.

References

[1] Samir Barra, Abdelghani Dendouga, Souhil Kouda, and Nour-Eddine Bouguechal, "Contribution to the Analysis and Modeling of the Non Ideal Effects of Pipelined ADCs using MATLAB", Journal of Circuits Systems and Computers, vol. 22, no. 2, Feb. 2013.

[2] J. Ruiz-Amaya, M. Delgado-Restituto, A. Rodrguez-Vazquez, “Behavioral modeling of pipeline ADC building blocks”, International Journal of Circuit Theory and Applications, vol. 40, no. 6, pp. 571-594, 2012.

[3] A. Dendouga, N. E. Bouguechal, S. Kouda, S. Barra, B. Lakehal, “Contribution to the modeling of a non-ideal Sigma-delta modulator”, Journal of Computational Electronics, vol. 11, no. 4, pp. 321-329, 2012.

[4] Piero Malcovati, Simona Brigati, Fabrizio Francesconi, Franco Maloberti, Paolo Cusinato and Andrea Baschirotto, “behavioral modeling of switched-capacitor sigma–delta modulators”, IEEE Transactions on Circuits and Systems - fundamental theory and applications, vol. 50, no. 3, march 2003.

[5] Xian Tang and Kong Pang Pun, A Novel Switched-Current Successive Approximation ADC, Journal of Circuits Systems, and Computers, 2011, vol. 20, no. 1, pp.15_27.

[6] Ying-Zu Lin, Chun-Cheng Liu, Guan-Ying Huang, A 9-Bit 150-MS/s Subrange ADC Based on SAR Architecture in 90-nm CMOS, IEEE Transactions on Circuits and Systems-I, vol. 60, no. 3, pp. 570–581, March 2013.

[7] Neena Nambiar, Benjamin J. Blalock and M. Nance Ericson, “A novel current-mode multi-channel integrating ADC”, Analog Integr Circ Sig Process, vol. 63, pp.283–291, 2010.

[8] Weibo Hu, Donald Y.C. Lie, and Yen-Ting Liu, “An 8-bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method”, IEEE Transactions on Circuits and Systems-I, vol. 60, no. 7, pp. 1726–1739, July 2013.

[9] Bard Haaheim_y and Timothy G. Constandinou, “A sub-1_W, 16kHz Current-Mode SAR-ADC for Single-Neuron Spike Recording”, in the proceeding of IEEE International Symposium on Circuit And Systems (ISCAS), 2012.

[10] S. Heydarzadeh, A. Kadivarian, and P. Torkzadeh, “Implemented 5-bit 125-MS/s Successive Approximation Register ADC on FPGA”, World Academy of Science, Engineering and Technology, vol. 69, pp. 394-397, 2012.

[11] R. Dlugosz and K. Iniewski, “Flexible architecture of ultra-low-power current-mode interleaved successive approximation analog-to-digital converter for wireless sensor networks”, VLSI Design, vol. 2007, no. 2, pp.1–13, 2007.

[12] Daniela DeVenuto, David Tio Castro, Youri Ponomarev, and Eduard Stikvoort, “0.8 mW 12-bitSAR ADC sensors interface for RFID applications”, Microelectronics Journal, vol.41, pp.746–751, 2010.

[13] Indrit Myderrizi, and Ali Zeki, “Behavioral Model of Segmented Current-Steering DAC by Using SIMULINK”, in the proceeding of Ph.D Research in Microelectronics and Electronics, , pp.156 – 159, 2009.

[14] Weibo Hu, Donald Y.C. Lie, and Yen-Ting Liu, An 8-bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method Vol. 4, NO. 3, pp. 17-22, Jan.-March issue (2011) , Journal on Electrical Engineering, special issue on “VLSI Design Methodologies/Embedded Systems”.

[15] Chung-Yi Li, Chih-Wen Lu, Hao-Tsun Chao, Chin Hsia ,A 10-Bit Area-Efficient SAR ADC with Re-usable Capacitive Array, The sixth IEEE International Conference on Anti-counterfeiting, Security, and Identification , 24-26 August