

Performance Enhancement of Static Transfer Switch Using Advanced State Estimation for Loss Minimization in Power Distribution Networks

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Abstract:

In modern power distribution networks, ensuring uninterrupted power supply with minimal losses is critical, especially for sensitive and critical loads. Static Transfer Switches (STS) play a key role in maintaining continuity by rapidly switching between two independent power sources during disturbances. However, conventional STS control strategies often rely on predefined thresholds and do not consider the dynamic state of the network, leading to inefficient switching and increased power losses. This paper proposes a novel approach to enhance the performance of STS by integrating advanced state estimation techniques. Using real-time estimation of voltage magnitudes, phase angles, and system stability indicators is performed. These estimated parameters are then used to intelligently control the switching operation of the STS, selecting the optimal source based on system health and expected power loss. A simulation model is developed in MATLAB/Simulink to evaluate the proposed method under various fault and load conditions. The results acquired demonstrated the competency of the proposed approach to endow improved voltage stability, reduced switching time, and significant minimization of power distribution losses as compared to traditional switching approaches. This work highlights the potential of state-estimation-based control in making STS operations more adaptive, reliable, and energy-efficient in smart distribution networks.

1. Introduction

In today's modern and dynamic power systems, endowing uninterrupted and efficient power delivery is a critical requirement, particularly for sensitive and high priority loads such as data centres, hospitals, and industrial processes. One of the key devices used to maintain power continuity is the Static Transfer Switch (STS), which facilitates rapid switching between two independent power sources in the event of a voltage sag, source failure, or quality degradation. Unlike traditional mechanical switches, STS operates using solid-state devices such as thyristors or IGBTs, enabling source transfer within a few milliseconds, thereby minimizing disruption [1]. However, traditional STS control mechanisms are primarily based on fixed threshold logic or local voltage/frequency

monitoring, which may not reflect the actual dynamic conditions of the network. Such static decision-making often results in unnecessary switching, delayed transfers, or even wrong source selection, ultimately increasing power distribution losses and reducing system efficiency [2]. To address these challenges, the integration of advanced state estimation techniques into STS control logic has emerged as a promising solution. State estimation provides real-time insight into the power system's internal conditions—such as bus voltages, phase angles, power flows, and line impedances—by processing available measurements through filtering and prediction algorithms. Techniques like the Kalman Filter and its variants enable accurate and robust estimation even in the presence of noisy or incomplete data. By embedding state estimation within the STS

control framework, the system can make more informed, predictive, and optimized switching decisions, not just based on voltage thresholds but also considering factors like source stability, load demand, and power loss minimization. This intelligent switching mechanism enhances the performance of STS, improves load reliability, and significantly reduces unnecessary energy losses in the power distribution network [3].

This study presents a simulation-based analysis of STS integrated with advanced state estimation, aiming to improve operational efficiency and minimize distribution losses. The proposed system is modelled and tested in MATLAB/Simulink under various loading and fault scenarios, and the results are compared with conventional switching methods to demonstrate its effectiveness [4-8]. Consider simple three-phase, balanced electric power distribution network consisting of two three-

phase voltage sources preferred and alternate connected to two different sending end voltage-buses VSP and VSA, respectively [9-10]. These sending-end buses are connected with receiving end buses through two different feeders namely preferred feeder and alternate feeder are connected. Fig.1. shows the single line diagram of the whole system. The two feeders have different impedances ' Z_{sP} ' and ' Z_{sA} ' and are connected at the far end to two different receiving-end voltage buses ' V_{PR} ' and ' V_{AR} ' respectively. This parallel feeder arrangement is made to improve power quality and reliability for the critical load. The critical load is mainly fed from the preferred feeder. The two different feeders alternatively supply electric power to the critical load connected to the load bus (VL) through static transfer switch (STS) [11-14]. Fig. 2 shows the structure of the preferred feeder system.

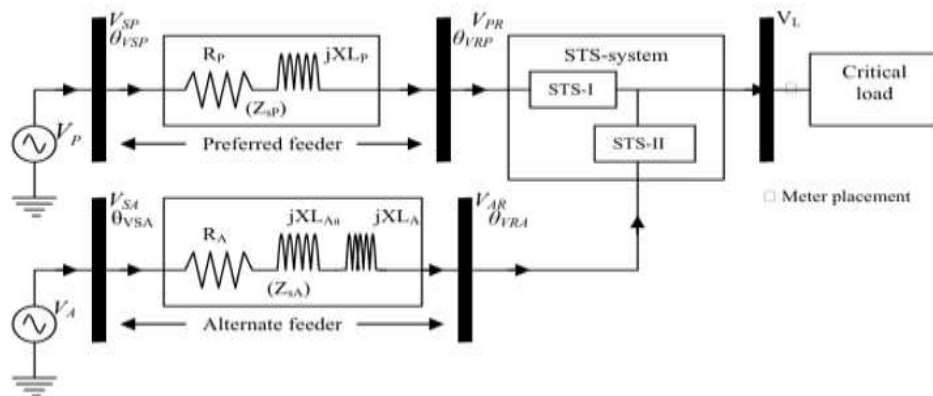


Figure 1. One-line diagram of two feeders-preferred and alternate, feeding sensitive load through STS: (A simplified distribution system model).

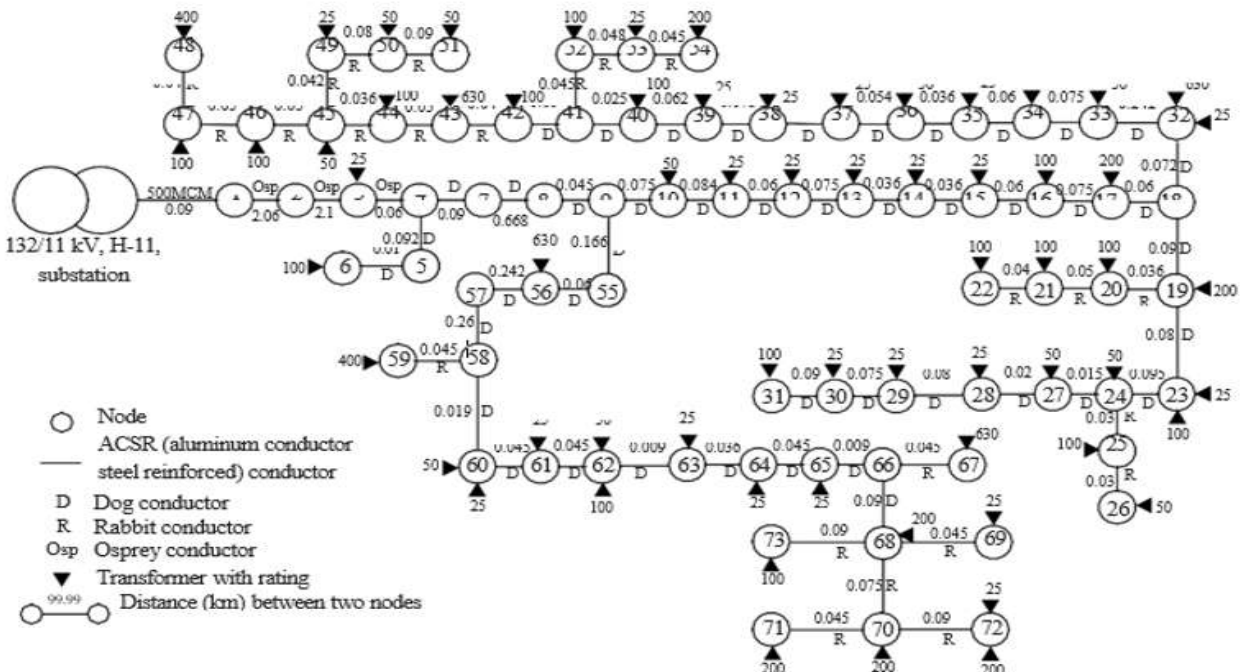


Figure 2. Online Diagram of Preferred feeder

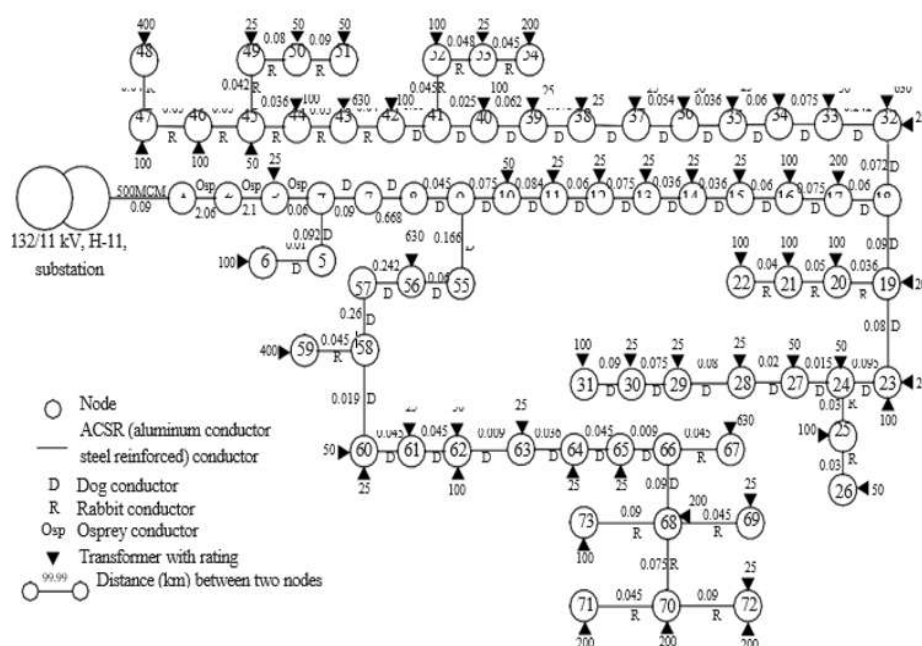


Figure 3 shows the online diagram of the alternate feeder of distribution system when fault occurs in preferred feeder power transfer to the alternate feeder by using Static transfer switch.

1. Static Transfer Switching System Structure

STS system consists of mainly two thyristor blocks and a control logic block. The structure of both STS blocks, i.e., block-I and block-II, is the same at the point of installation, as shown in Fig.3. Each STS block has two thyristors per phase connected back-to-back to allow load current to flow in both positive and negative directions [15].

STS-block-I

This block is connected in series with the preferred feeder and is normally ON, i.e., the load is fed from the preferred feeder. The control logic block generates the required gate pulses for the respective

thyristors of this block to turn it ON.

STS-block-II

This block is connected across both the feeders, preferred and alternate, and is normally OFF, i.e., no gate pulse is applied by the control logic block to turn it ON. When the preferred feeder is overloaded, the control logic block detects a voltage sag at the point of installation (PoI) of the STS and generates a high gate signal to turn ON the thyristors of STS-block-II.

At the same time, the control logic generates a low gate signal for the thyristors of STS-block-I. Ultimately, STS-block-II is turned ON and STS-block-I is turned OFF. Hence the sensitive load of the preferred feeder is now fed by the alternate feeder [16]. Fig. 4 shows the schematic diagram of preferred and alternate feeder with normal, sensitive load and STS blocks.

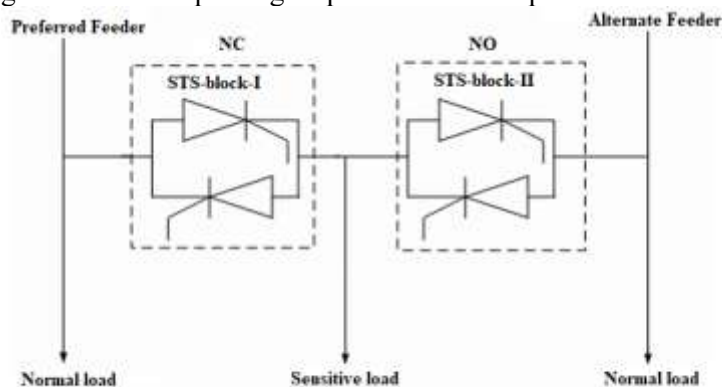


Figure 4. Schematic diagram of preferred and alternate feeder with normal, sensitive load and STS blocks.

The control logic of the STS-system performs load transfer when needed to the alternate feeder and

back when fault or disturbance is removed. The main purpose for the installation of STS in the distribution network is to provide uninterruptible power to the sensitive load that shown in Fig.5. However, when the sensitive load demand is constant and hence its power factor is also constant, then the operation of the STS's control logic for transferring of load from the preferred feeder to the alternate feeder and vice versa is simple. In case of

fixed power factor, a fixed delay in the firing pulse of incoming thyristors will serve the purpose and transfer of load from preferred feeder to alternate feeder will take place without any cross current. However, the situation is complicated in case of varying load, due to variation in the power factor. It becomes difficult to predict the amount of delay in the firing pulse in real time for the thyristors of STS blocks.

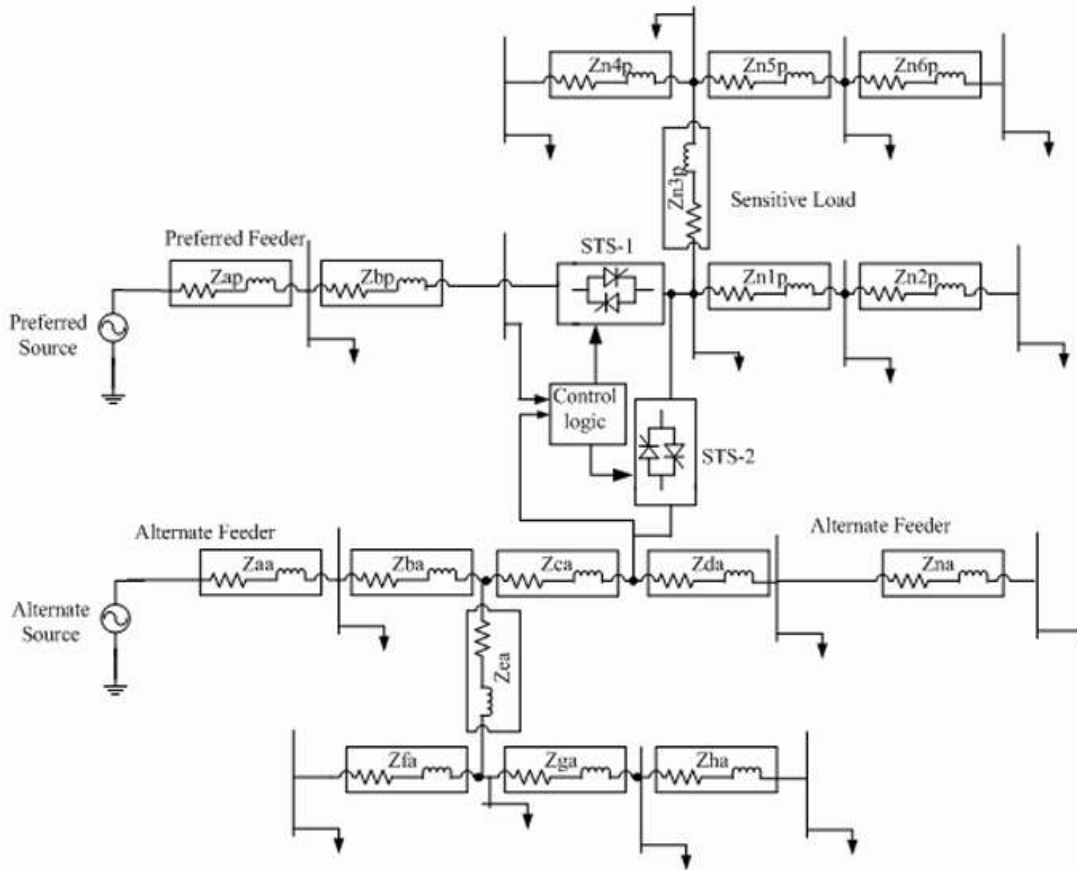


Figure 5. Schematic diagram of preferred, alternate feeder, and STS-system

2. Advanced State Estimation Approach

Advance State estimation is the process of assigning a value to an unknown system state variable based on measurements from that system according to some criteria

The state variables are taken as the bus voltage magnitudes and relative phase **angles**, but the reference bus voltage angle is set to zero [17]. State estimation process involves the following functions [18]:

Network topology analysis: This is used to determine the real time network structure based on digital measurements.

Observability analysis: This is used to determine whether the system is observable based on the available analog measurements. If the system is not-**observable**, then pseudo-measurements will be added to make the system observable. Only

observable parts of the system can be estimated.

State estimation computation: This is used to estimate the state of the system according to the usable measurements. The state estimation computation encompasses the bad data detection and identification process, Bad data detection and identification: This is used to detect and identify bad data in the measurement set based on the analysis of measurement residuals. If any bad data are detected, it will be removed from **the measurement** set and state estimation will be repeated [18]. The problem of state estimation is constituted by an over-determined system of non-linear equations i.e. when number of measurements (N_m) is greater than the number of unknown parameters being estimated (N_h). The problem of state estimation may also be either completely determined when $N_m = N$, or under-determined when N_m is less than N . The mathematical model

of WLS state estimation can be derived from different mathematical relations between measurements and state variables [19]. The model relates the measured values of the monitored variables with the state **variables such** as:

$$z = h(x) + I \quad (1)$$

z : Measurement vector ($m \times 1$)

$h(x)$: Nonlinear function vector ($m \times 1$)

x : True system state vector ($n \times 1$)

I : Measurement error vector ($m \times 1$)

Error Assumptions:

$$E[i] = 0$$

$$E[i i^T] = R \quad (2)$$

Where R is the noise covariance matrix:

$$R = \begin{bmatrix} \sigma_1^2 & 0 & \dots & 0 \\ 0 & \sigma_2^2 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & \sigma_m^2 \end{bmatrix}$$

$$R = \text{diag}(\sigma_1^2, \sigma_2^2, \dots, \sigma_m^2)$$

Advance state Estimation Objective:

$$\text{Minimize } J(x) = \sum [r_i / \sigma_i]^2 \quad (3)$$

Or in matrix form:

$$J(x) = [z - h(x)]^T R^{-1} [z - h(x)] \quad (4)$$

Optimality Condition:

$$\partial J(x) / \partial x = 0$$

$$H(x) = \partial h(x) / \partial x \text{ (Jacobian)}$$

Jacobian matrix of the measurement function $h(x)$.

$$\text{Then, } H^T(x) R^{-1} [z - h(x)] = 0 \quad (5)$$

Iterative Update Equation

Given the iteration index k , the update rule is:

$$x_{k+1} = x_k + \Delta x_k \quad (6)$$

where the update increment Δx_k satisfies the equation:

$$G(x_k) \Delta x_k = H^T(x_k) R^{-1} [z - h(x_k)] \quad (7)$$

Description of Terms

- x_k : State vector at iteration k
- Δx_k : Incremental update to the state
- $G(x_k)$: Gain matrix (often a Jacobian or approximation)
- $H^T(x_k)$: Transpose of the observation Jacobian at x_k
- R : Covariance matrix of observation noise
- $[z]$: Observation vector
- $h(x_k)$: Nonlinear observation model evaluated at x_k

3. Se Technique Implementation For Impedance Matching

In this paper, an advance State Estimation technique has been used for estimating the bus voltages and their angles. To solve the problem of cross current during switching operation of STS

from faulty (preferred) feeder to healthy (alternate) feeder, Advance state estimation technique has been implemented for matching the impedance difference between both feeders. The difference of impedance cause phase angle difference between both buses at the STS input terminals. Due to this phase difference, cross current flows in the system and source parallel occurs and hence STS transfer time increases. To overcome the phenomena of cross current, the voltage phase angles at STS terminal must be known using some measuring instruments. But the readings are not always accurate due some errors in the instrument, so estimation of these parameters becomes necessary [20].

4. Problem Formulation

For our problem, firstly, estimation of bus angles ($\angle V_{r1}$, $\angle V_{o1}$, $\angle V_{r2}$) has been made. Secondly, the shunt capacitor value will be calculated. By placing the shunt capacitor along the alternate feeder, the phase difference can be minimized. When there is no phase difference, or zero phase difference, between buses at the STS terminal, then during switching operation, no cross current will flow [19-20]. Hence, we can say that both feeder impedances have been matched. For a simple case study, consider the following data:

$$|V_{s1}| = 1.0 \text{ p.u.}$$

$$|V_{s2}| = 1.0 \text{ p.u.}$$

$$\angle V_{s1} = 0^\circ \text{ (taken as reference angle), } \angle V_{s2} = 0^\circ$$

$$|V_{r2}| > 0.95 \text{ p.u., and } \angle V_{r1} = 0, \text{ otherwise } |V_{r2}| >$$

0.95 p.u. because standby source is always available

X_1 = Reactance of preferred feeder between buses V_{s1} and $V_{r1} = 0.2 \text{ p.u.}$

X_2 = Reactance of alternate feeder between buses V_{s2} and $V_{r2} = 0.3 \text{ p.u.}$

$$\sigma = \text{Meter standard deviation} = 0.01 \text{ p.u.}$$

$$\text{Base power} = 100 \text{ MW}$$

$$\text{Base MVA} = 100 \text{ MVA}$$

5. Case Study & Result Discussion

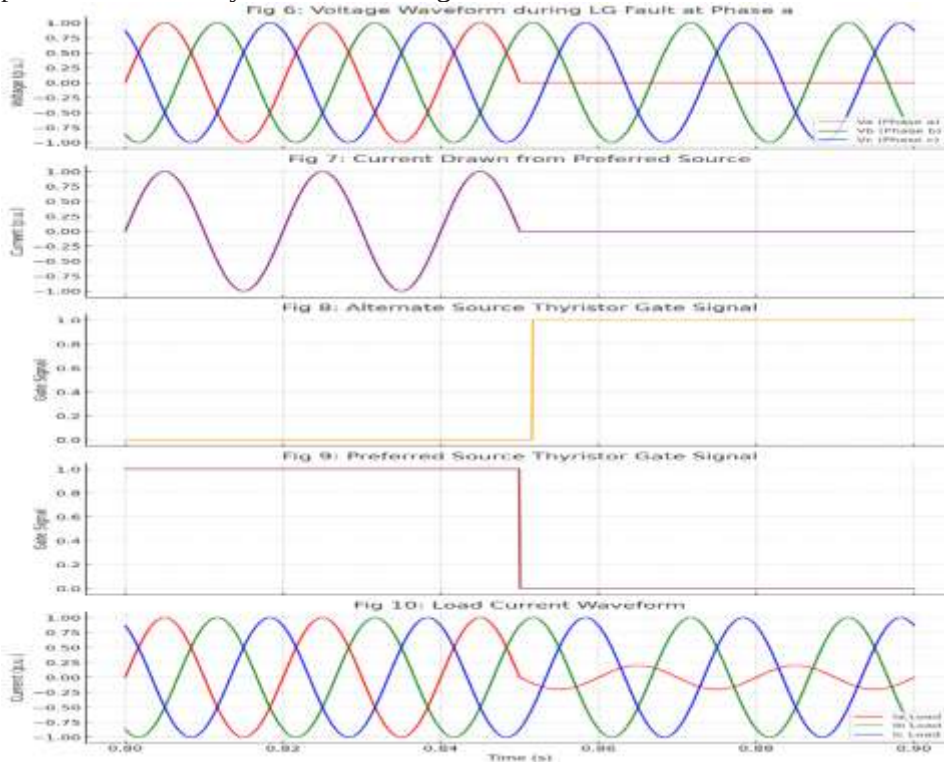
Different disturbances are generated at preferred source to check the behavior of static transfer switch.

A. Line to Ground fault at Phase “a”

When there is line to ground fault at phase “a” at time 0.85 sec. Fault detection time is about 1.6ms and transfer time is about 4ms. Voltage waveforms of three phases are given in fig 6. As fault occurs at phase “a” voltage magnitude becomes zero which is clearly observed. Fig.7. shows the Current drawn from preferred source. When fault occurs there is a delay of about 1.6ms during which the thyristors of

preferred source is completely turned off and thyristors of alternate source are turned on to feed the load. Fig 8 shows the turning on and off signal of alternate source thyristor. When the preferred source thyristors are turned on before occurrence of fault, thyristors of alternate source have gate signal of zero magnitude. Fig.9. shows the gate signal fed to the thyristors of preferred source. Gate signal of preferred source thyristors has a magnitude of one

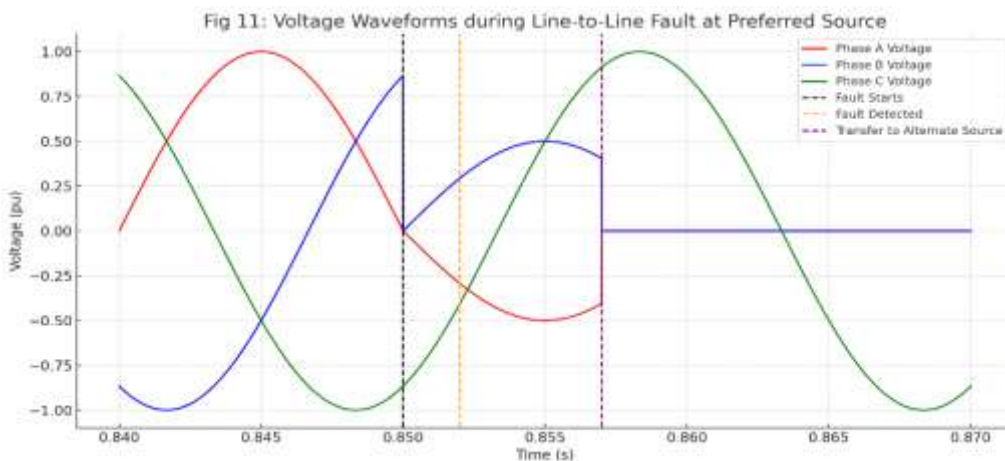
when static transfer switch system detects no disturbance in the system. Fig.10.shows When fault occurs at 0.85 sec static transfer switch system detects this fault and signal is removed from preferred source thyristors and fed to alternate source thyristors. Load current waveform. Small variation in the current magnitude of phase “a”.



B. Line to Line Fault at Phase a & b

In this case, three phase static transfer switch behavior is discussed when line to line fault occurs on preferred source at 0.85 sec. Fault is detected at 0.852 sec and the transfer of load to alternate source is at 0.857 sec so total transfer time is 5ms. Fig 11 shows the clear picture of system behavior when there is line to line fault on the system. It is clearly shown from Fig 11 that disturbance is more severe

in line-to-line fault cases as compared to line to ground fault, so static transfer switch system takes more time to shift load from preferred source to alternate source. This shows that detection time greatly depends on the point on the wave where fault is started and also on other parameters like filter parameters and difference in feeder impedances.



C. Three Phase Short Circuit Fault

Static transfer switch transfers load from preferred source to alternate source when there is three phase short circuit fault at preferred source. When a fault occurs at 0.85 sec voltage detection module detects faults and generates transfer signal to gating logic module which turns off the thyristors of preferred source and turns on thyristors of alternate source. The detection time of three phase fault shows in fig.12. is 2ms approximately and transfer time is approximately 6ms so total transfer time of load

from preferred source to alternate source is about 8ms. Fig 12 shows the preferred source voltage before, after and during three phase faults. It is clearly that when a fault occurs preferred source voltage becomes zero while before and after fault it supplies power at its rated voltage. load current during three phase faults at preferred source. It is clearly observed from results that static transfer switch efficiently transfers load during fault condition with very minimum time and without any interruption to load.

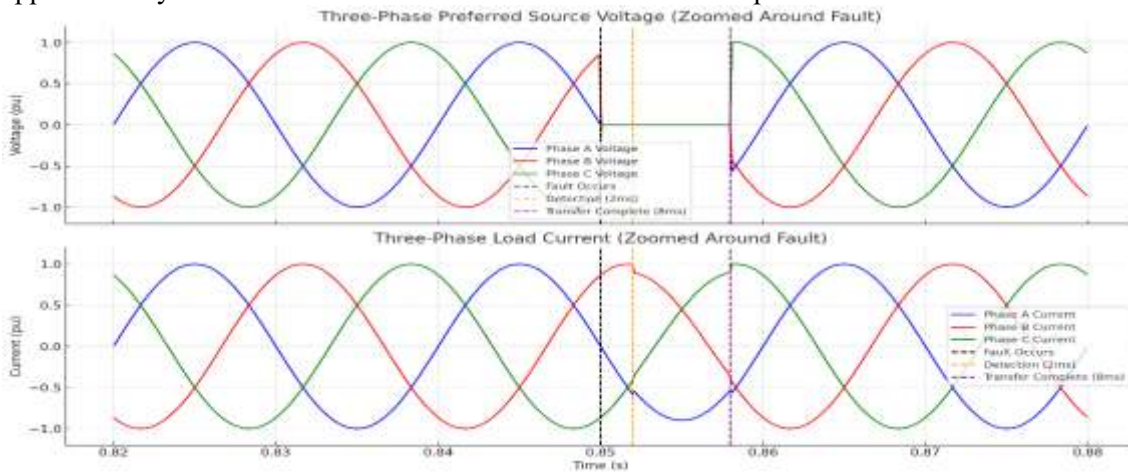


Figure 12. source voltage before, after and during three phase faults

Transfer times of static transfer switch during different disturbances are summarized in this section. Transfer times with disturbances are given below in the Table 1.

Table 1. Transfer times with disturbances

Case no.	Type of Fault on preferred source side	Detection Time(ms)	Transfer Time (ms)	Total Transfer Time(ms)
1.	L-G Fault at phase 'a'	1.6	2.4	4.0
2.	L-L Fault at phase 'a & b'	2.0	3.0	5.0
3.	Three phase Fault	2.0	6.0	8.0

Now, the phase angles (i.e., $\angle V_{r1}$, $\angle V_{r2}$) at both receiving end buses have been estimated. The estimated values of both angles were found to be 87.7° and 84.8° , respectively. Thus, the total phase angle difference is 2.9° . Then, the power factor correcting. Factor will be 0.142 [17-20]. To eliminate this phase difference and to match the impedance difference between both feeders, the value of shunt capacitor is found as follows: Suppose the critical load of 5500 kW, having power factor of 0.92 lagging is fed by the preferred feeder. The value of shunt capacitor calculated as 6.8 micro

farad (781 kVAR). This 6.8 micro farad was connected along the alternate feeder and again the circuit of Fig. 1 was simulated. The result shows that there is no cross current in the system and shows that transfer time has also been minimized and different types of faults analysis has been done & power transfer to the load continuously with minimum time delay.

6. Conclusion

This paper gives a complete simulation study of thyristor based static transfer switch system. A Simulink based model is developed to analyze the performance of static transfer switch. An efficient voltage detection scheme and control strategy is presented in this paper for the fast transfer of sensitive load from preferred source to alternate source. Different types of disturbances are generated to observe the performance of static transfer switch system. Transfer time determined from commutation process between thyristor switches greatly relies on control strategy of static transfer switch, system parameters and disturbance characteristics. Transfer time during different disturbance conditions are less than other systems designed by different researchers which shows the efficient performance of static transfer switch systems. Advance state estimation techniques have been implemented to match the feeder impedances

of the two complementary feeders to improve the reliability and quality of power. Fast service restoration through feeder reconfiguration and minimization of the losses. The significance of static transfer switch has been highlighted for the smooth transfer of sensitive loads from one preferred sources/feeder to another alternate source/feeder when fault/disturbance occurs at the preferred source/feeder. The structure of proposed STS-system and its control logic have been explained in detail. Different types of switches used in power distribution system have been explained. MAT-LAB professional software has been used for simulation of different test circuits.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
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- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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