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Research Article

Non-Periodic Current Regulation in Digitally Controlled Hysteresis Current Controller

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Abstract:

This paper investigates the challenges associated with non-periodic current tracking in digitally controlled Hysteresis Current Controllers (HCC) within grid-connected inverter systems. It examines the dynamic response of the controller when the grid phase undergoes variations, leading to deviations in current tracking. The study explores how phase shifts influence the accuracy of current regulation and their impact on overall system performance. A key aspect of the analysis is the evaluation of total harmonic distortion (THD) in the inverter's output current, which serves as a critical parameter in assessing grid connection quality and harmonic mitigation.The research employs MATLAB/Simulink simulations environment to analyse the behaviour of the inverter under different grid conditions. The results highlight the difficulties posed by phase variations and their effect on maintaining precise current regulation. Furthermore, the study identifies potential limitations of HCC in ensuring consistent performance under fluctuating grid scenarios. The observed non-periodicity in current tracking suggests the need for controller optimization to enhance synchronization and minimize harmonic distortions. The insights derived from this study contribute to the refinement of digital HCC techniques, aiming to improve inverter efficiency and grid compatibility. By addressing the challenges associated with phase shifts and THD, the findings offer valuable guidance for designing more robust current control strategies in grid-connected applications.

1. Introduction

Current control in single-phase inverters has been a fundamental topic in power electronics for several decades. The principles governing single-phase inverter operation also play a crucial role in the development and control of three-phase inverters. Efficient current regulation is essential for maintaining power quality, reducing harmonic distortion, and ensuring stable inverter performance. **Inverter systems commonly employ three current control strategies: Hysteresis Current Control (HCC), Ramp Comparator Current Control (RCCC), and Predictive Current Control (PCC).**Hysteresis Current Control is a simple and fast-responding method that maintains current within a predefined band by switching the power devices accordingly. Although it offers rapid dynamic response, it has drawbacks such as variable switching frequency, which can introduce additional harmonics in the system. Ramp Comparator Current Control operates by comparing the actual current with a reference signal using a ramp waveform. This technique provides more uniform switching frequency compared to HCC, improving system predictability. However, its performance may be affected by system delays and parameter variations. Predictive Current Control, on the other hand, utilizes a mathematical model of the inverter to predict future current values based on system dynamics. It adjusts the switching states accordingly to minimize current error. This technique offers high accuracy and better harmonic performance but requires intensive computational

resources for real-time implementation. Each of these control methods has its advantages and limitations, and their selection depends on the specific application requirements, such as response speed, harmonic performance, and implementation complexity [1]-[3]. Hysteresis Current Control (HCC) is a nonlinear control strategy frequently implemented in power electronic converters. It operates by maintaining the current within a defined hysteresis band, ensuring rapid dynamic response and precise current regulation. High-power converters operate at a finite switching frequency, which is constrained by the characteristics of semiconductor devices. These devices have specific limitations concerning their maximum and minimum switching frequencies, as outlined in various studies [3]-[6]. Maintaining the converter's operation within an appropriate frequency range is crucial to minimizing switching losses and ensuring efficient performance. Excessive switching frequency can lead to increased power losses and thermal stress on semiconductor components, whereas excessively low switching frequency may result in degraded current regulation and poor dynamic response. Therefore, determining the appropriate operating frequency during the design stage is essential for optimizing system efficiency and reliability.By accurately predicting the switching frequency, designers can ensure stable operation while minimizing losses associated with frequent switching events. Various analytical and simulation-based approaches are available to estimate the operating frequency, helping engineers make informed decisions in the early stages of system design. Ultimately, selecting an optimal frequency range improves the overall performance, enhances the lifespan of semiconductor components, and reduces energy losses in high-power applications.

The main purpose of the PWM technique is to get Sinusoidal current, which will provide the constant torque to any Electric drives, less harmonic losses in the converter output side, efficiency is more [6]-[8]. That's why PWM scheme is very popular, in this paper a hysteresis current type control isanalyzed with the effect of switching time or sampling frequency on the switching frequency [9]. The purpose of the PWM is to have a nearly sinusoidal current so even though controlling the voltage [10]. So, the current is nearly sinusoidal and the harmonics are shifted to high frequencies. So, in current hysteresis controlled PWM, nearly generated sinusoidal current or the output current waveform. Sampled Pulse Width Modulation (PWM) is an analog technique where the input signal is sampled using a carrier signal [7]. The hysteresis band h is implemented to maintain the current ripple within specified limits, ensuring it does not exceed or drop below the set range. This band also regulates the switching behavior of the power device. Given the system's nonlinear nature, the hysteresis current control method demonstrates significant effectiveness. It offers advantages such as rapid dynamic response, superior current tracking capability, structural simplicity, and enhanced robustness. These attributes make it particularly suitable for applications requiring precise current regulation. The time-domain behavior of a grid-connected system utilizing an analog-controlled hysteresis current control technique has been thoroughly examined. Analyzing the time-domain formulation of the hysteresis controller in a grid-connected setup offers valuable insights into its performance across different grid conditions. This analysis considers different operating modes based on the phase difference between the grid voltage and the reference current [9]-[12]. The ability of hysteresis current control to maintain stability and accuracy in current tracking makes it a reliable approach for grid-connected applications. By ensuring high-speed response and effective current regulation, this technique remains a widely used method for improving power quality in grid-connected systems and power electronic applications.

A generalized relationship is established between the sampling time (or sampling frequency) and the operating time (or operating frequency) to analyse the impact of sampling frequency on the operating frequency in a hysteresis current-controlled (HCC) single-phase inverter. This inverter is integrated into the grid, and further details can be found in references [1]-[2], [13].

This study focuses on the non-periodicity observed in current tracking when implementing a digitally controlled HCC. The current waveform within the hysteresis band exhibits irregularities due to the interaction between switching frequency modulation and sampling frequency variations. Unlike traditional analog HCC, where switching frequency dynamically adjusts based on system conditions, digital implementation introduces discrete control actions,

leading to non-uniform switching intervals. These variations disrupt the expected periodic behavior of the current, causing fluctuations in the switching pattern. Furthermore, the effect of sampling frequency on current regulation is examined, revealing that lower sampling rates result in larger deviations within the hysteresis band, whereas higher sampling frequencies contribute to more stable yet computationally

demanding control. The study highlights the trade-offs between computational complexity and current tracking accuracy in digital HCC applications. By analyzing the dynamic behavior of the inverter in a grid-connected scenario, this research provides insights into optimizing the sampling frequency to minimize non-periodicity and enhance overall system performance. The findings contribute to the refinement of digitally controlled hysteresis current controllers, ensuring improved stability and efficiency in power electronic applications.

2. Hysteresis current control

In Hysteresis current control scheme the main purpose is to generate the sinusoidal current. In this PWM is used so that the current ripple is confined into a Hysteresis band [1], [3], [10]. So that average variation of the current is near about sinusoidal. The switching of the device is done by introducing a envelop along the reference current. The single phase two level full bridge Voltage source inverter with Grid Connected System is show in the Figure l.This bridge is consisting S_l, S_2, S_3 and S_4 in MOSFET. Where $S_4$and S_l are in same leg where$S_2$and $S_3$are in the same leg and S_l and S_2, S_3 and S_4 are operating 180-degree phase shift respectively [2], [6], [8], [14]. The inverter output is connected to the resistance *R* and inductance *L* whose *R* value is very small, and the switching frequency depends upon the value of *L*. And grid or motor as a load. The $i = i_L$current which is the instantaneous in nature is compared to the i_{Lref} current and this will generate the error. This error signal is passes through the Hysteresis band as shown in Figure 1.

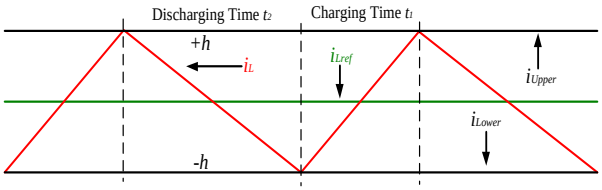

Figure 1 *Switching of a Device according to Envelop*

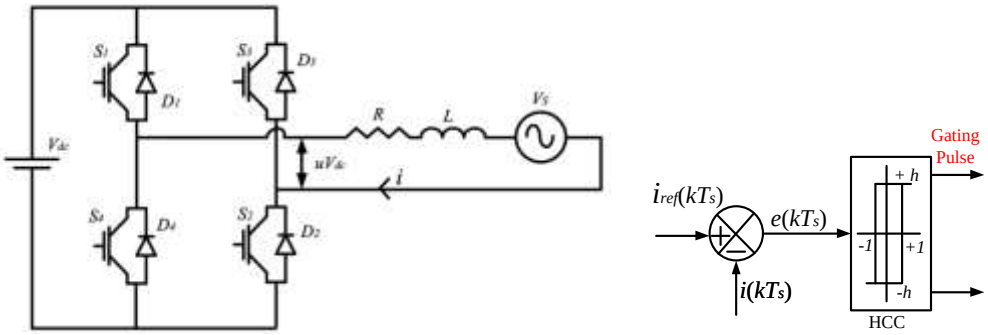

Figure 2 *Single Phase Voltage Source Inverter with Grid connected System*

In this inverter, a fixed-band hysteresis current control technique is employed to regulate the load current (i_{act}) and maintain a sinusoidal waveform. The hysteresis band plays a crucial role in generating gate signals, which subsequently produce the PWM output. By continuously monitoring the actual current and adjusting the switching states accordingly, the controller ensures that the current remains within the predefined hysteresis band. This method effectively minimizes current distortions and enhances system performance. The fixed-band approach offers simplicity, fast dynamic response, and effective tracking of the reference signal, making it a reliable choice for power electronics applications.

$$e > +h, u = +1, V_O = +V_{dc} \quad (1)$$

$$e < -h, u = -1, V_O = -V_{dc} \quad (2)$$

where, $e = i_{Lref} - i_L$, and *h* is Hysteresis band which is shown in Figure 2(b).Now, when error signal is passes through Hysteresis current controller and it generates the gate signal for the Voltage Source Inverter. The dynamic equation of this Inverter shown in Figure 2. can be written as:

Using (1), and (2), taking $V_S = 0$.

$$\frac{di_L}{dt} = \frac{V_{dc}}{L} - \frac{Ri_L}{L} \quad (3)$$

$$\frac{di_L}{dt} = -\frac{V_{dc}}{L} - \frac{Ri_L}{L} \quad (4)$$

For negative slope: $e^- = i_{Lref} - i_L^+$ and

For positive slope: $e^+ = i_{Lref} - i_L^-$

Therefore, the rate of change of the error (Δe) is defined under two specific conditions as outlined below.

- During charging time

$$\frac{de^-}{dt}t_1 = -2h \quad (5)$$

- During discharging time

$$\frac{de^+}{dt}t_2 = +2h \quad (6)$$

Heret_1 and t_2 represent the total durations of the charging and discharging phases, respectively, for an ideal Hysteresis Current Controller, as illustrated in Figure 1.Assume the system aims for the i_L, to follow a reference current a i_{Lref}. This behavior depends on both the DC supply and the load. To manage this, a hysteresis band is introduced after the comparison stage. Expanding this band defines upper and lower limits for i_L,denoted as $i_{upper}$and i_{lower}; which in turn govern the switching of the device [4]-[8].When switches S_1 and $S_2$are turned on, the i_L increases from i_{lower} to i_{upper}, and when switches S3 and S4 are activated, $i_L$decreases from $i_{upper}$to i_{lower}, as illustrated in Figure 1.The generalized equation for the Charging and Discharging time is when grid is connected to the system with grid voltage is V_{grid} where the effect of the resistance R is neglected due to the very small value are [15]-[17]:

$$t_1 = \frac{\Delta I}{\left[\frac{V_{dc/2}}{L} - \frac{V_{grid}}{L}\right]} \quad (7)$$

and

$$t_2 = \frac{\Delta I}{\left[\frac{V_{dc/2}}{L} + \frac{V_{grid}}{L}\right]} \quad (8)$$

Also, and are called as t_{on} and t_{off} respectively. Then switching time $t_s$is equal to sum of the t_1 and t_2. So,

$$t_s = \frac{L\Delta I V_{dc}}{\left[\left(V_{dc/2}\right)^2 - \left(V_{grid}\right)^2\right]} \quad (9)$$

It means switching frequency

$$f_s = \frac{\left[\left(V_{dc/2}\right)^2 - \left(V_{grid}\right)^2\right]}{L\Delta I V_{dc}} \quad (10)$$

For an Inverter Input voltage $V_{dc/2}$ is fixed ,$V_{grid}$is fixed and L is fixed, it means f_s is totally depends up on the $\frac{1}{\Delta I}$.

$$\Delta I = \frac{\left[\left(V_{dc/2}\right)^2 - \left(V_{grid}\right)^2\right]}{f_s L V_{dc}} \quad (11)$$

from equation (10) f_{smax} is obtained and that is:

$$f_{smax} = \frac{V_{dc}}{4hL} \quad (11)$$

In a fixed hysteresis band control strategy, the band limit is influenced by key factors such as switching frequency, supply voltage, and the inductance (L) of the circuit. The switching frequency determines how frequently the controller adjusts the current, while the supply voltage affects the rate of change of current. Additionally, the inductance plays a crucial role in shaping the system's response, as it dictates the rate at which current can vary. Similarly, From equation (10) $f_{smin}$is obtained and that is:

$$f_{smin} = f_{s\max}\left[1 - \left(\frac{V_{grid}}{V_{dc/2}}\right)^2\right] \quad (12)$$

And

From equation (10) $f_{savg}$is obtained and that is:

$$f_{savg} = f_{s\max}\left[1 - \frac{1}{2}\left(\frac{V_{grid}}{V_{dc/2}}\right)^2\right] \quad (13)$$

And for a Sinusoidally varying V_{grid} voltage.

$$V_{grid} = mV_{dc/2}\sin wt \quad (14)$$

Where, m is the modulating index

So,

$$f_s = f_{s\max}\left[1-m^2\sin^2 wt\right] \quad (15)$$

This equation (14) give information about the switching frequency which varies for a fixed Hysteresis band.

$$f_s = f_{s\max}\left[1-\frac{m^2}{2}+\frac{m^2}{2}\cos 2wt\right] \quad (16)$$

f_s is varies around an average value which is given in the equation (13).When the hysteresis current control (HCC) structure is applied digitally, the charging and discharging times of the current are influenced by the sampling time. Unlike analog implementations, where the switching occurs continuously based on instantaneous current values, digital control introduces a delay due to the discrete nature of sampling. This delay affects the rise and fall times of the current error, impacting the overall performance of the system.To examine this effect, the system's response is assessed by observing the rise and fall times of the current error. These parameters provide insight into how quickly the system reacts to changes in current demand and how efficiently the controller maintains the desired reference current. As shown in Figure 4, the finite sampling time introduces non-periodicity in current tracking, causing variations in switching frequency and potentially increasing current ripple. This evaluation is crucial for optimizing the digital

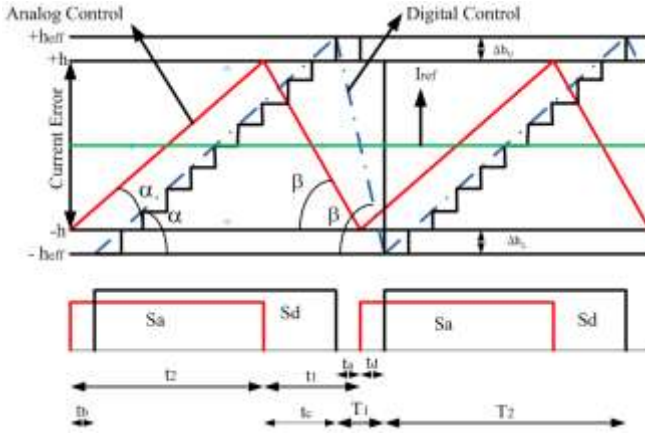

Figure 4 *Rise time and Fall time of Digital Control [1]*

implementation of HCC, as it helps in selecting appropriate sampling intervals to minimize deviations in current tracking. By carefully tuning the sampling rate, the adverse effects of digital control on current dynamics can be mitigated, improving the stability and performance of the hysteresis current control scheme in various power electronics applications.

$$T_1 = t_1 + t_b + t_c \quad (17)$$

$$T_2 = t_2 + t_a + t_d \quad (18)$$

Where,

$$\alpha = tan^{-1}\left(\frac{2h}{t_2}\right)$$

and

$$\beta = tan^{-1}\left(\frac{2h}{t_1}\right)$$

so, from the Figure 4.

$$T_1 = t_1 + \frac{t_1}{2h}\left(\Delta h_l + \Delta h_u\right) \quad (19)$$

$$T_2 = t_2 + \frac{t_2}{2h}\left(\Delta h_l + \Delta h_u\right) \quad (20)$$

Using equations (17) and (18), the switching period of the digital controller can be determined as follows:

$$T_{sd} = T_1 + T_2 \quad (21)$$

The variable Δt represents the relationship between the switching periods of the analog and digital controllers.

$$\Delta t = \left(1+\frac{1}{2h}\left(\Delta h_l + \Delta h_u\right)\right) \quad (22)$$

In a digitally implemented Hysteresis Current Controller (HCC), the delay time Δ*t*arises due to the sampling time. The values of $\Delta h_l$and Δh_u are influenced by the parameters α and β [1]. When designing an HCC, it is essential to ensure that the actual current (i_{act}) remains within the hysteresis band.Sampling is the technique of obtaining discrete-time values from a continuous-time signal by capturing its instantaneous amplitudes at specific intervals. A sample is a subset extracted from continuous-time data at specific intervals. In analysing the i_{act}, it is observed that the frequency of the rippled load current exhibits non-periodicity.

This phenomenon arises due to the fixed sampling frequency, which results in variations in the switching frequency.The switching frequency fluctuates between its minimum and maximum values. This variation is a direct consequence of the constant sampling frequency, which modulates the switching frequency. As a result, the frequency of the load current does not remain periodic, leading to non-uniform current tracking. The modulation of switching frequency on the sampling frequency introduces irregularities in the current waveform, affecting system performance.This non-periodicity poses a challenge in ensuring smooth current tracking, as the dynamic nature of the hysteresis band and switching frequency variations cause deviations in expected performance. Proper tuning of sampling and control parameters is necessary to minimize these effects and achieve improved current regulation. By optimizing the design of the HCC, it is possible to reduce switching frequency variations and improve the overall efficiency of digitally controlled power converters.

3. Simulation parameter

Parameter	Value
DCSourceVoltage,$V_{dc}/2$	40V
Resistance (R),Inductance (L)	1Ω, 10mH
Fundamental Frequency	50Hz
Grid Supply Voltage	$25V_{rms}$
Reference Current (i_{ref})	$4.0A_{max}$

4. Simulation results

After simulating the model at three different sampling frequencies (10 kHz, 100 kHz, and 1000 kHz) while maintaining a maximum switching frequency of 10 kHz, the results are illustrated in Figures 5–10. It is evident from Figures 6 and 8 that the load current exhibits ripples that exceed the hysteresis band boundary when the switching time is 100 times shorter than the sampling time. Similarly, Figure 10 shows the presence of ripples in the load current, but they remain within the hysteresis band limits. This behaviour can be attributed to the delay introduced during the analog-to-digital (A/D) and subsequent digital-to-analog (D/A) conversion processes.To mitigate this delay, a high-speed controller is necessary when implementing the Hysteresis Current Controller (HCC) digitally. A fast-operating controller helps maintain the accuracy and stability of the current tracking process by reducing conversion-related delays. Moreover, Figures 5, 7, and 8 indicate an asymmetrical distribution of switching frequency in the positive half-cycle of the load current. However, an odd symmetry can be observed in the switching frequency across the positive and negative half-cycles of the load current. This suggests that while the switching behaviour may be inconsistent in one half-cycle, an overall symmetrical pattern emerges when both halves are considered together. These findings highlight the challenges in digitally implementing HCC and emphasize the importance of optimizing controller speed to minimize delays and improve current tracking accuracy.

CASE I: SAMPLED FREQUENCY = 10KHZ

Maximum SWITCHINGFREQUENCY = 10KHz

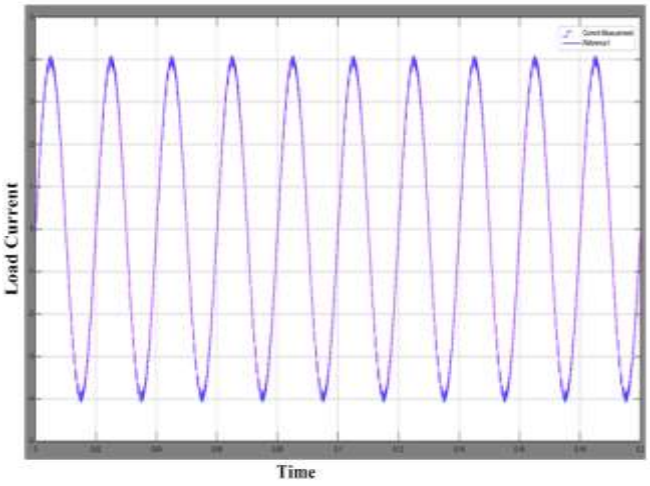

Figure 5 *Inverter Output Current at f_{sd} = 10KHz*

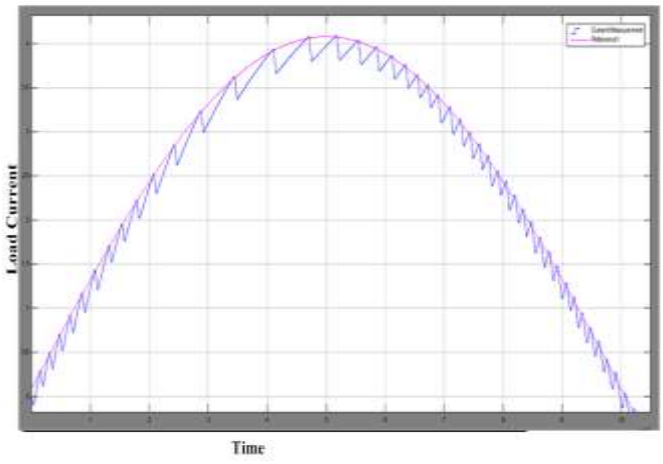

Figure 6 *Zoom in Inverter Output Current at f_{sd} = 10KHz*

CASE II: : SAMPLED FREQUENCY = 100KHZ

Maximum SWITCHING FREQUENCY = 10KHz

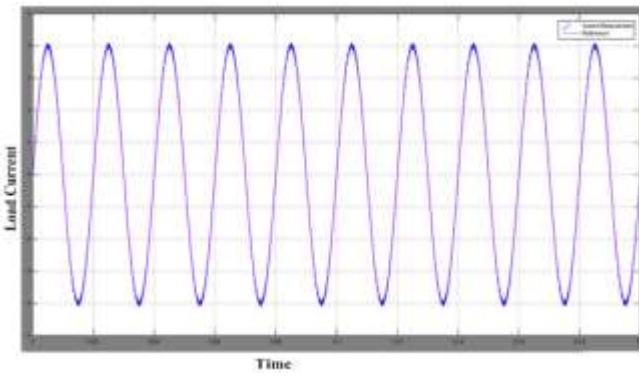

Figure 7 *Inverter Output Current at f_{sd} = 100KHz*

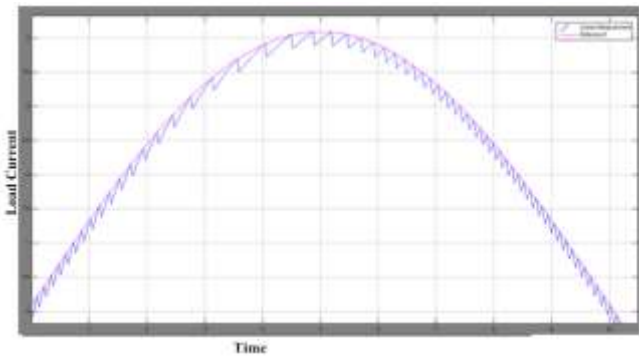

Figure 8 *Zoom in Inverter Output Current at f_{sd} = 100KHz*

CASE III: : SAMPLED FREQUENCY = 1000KHZ

Maximum SWITCHING FREQUENCY = 10KHz

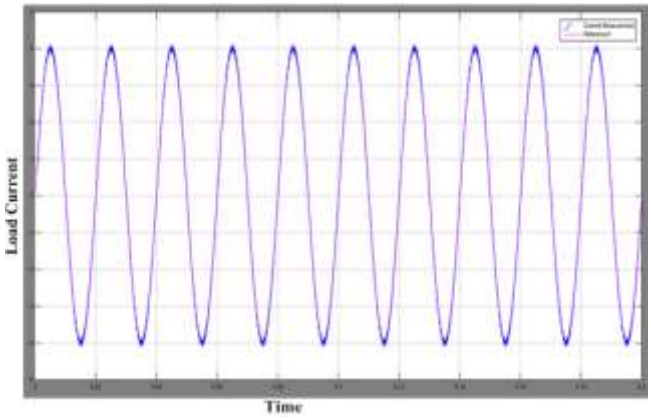

Figure 9 *Inverter Output Current at f_{sd} = 1000KHz*

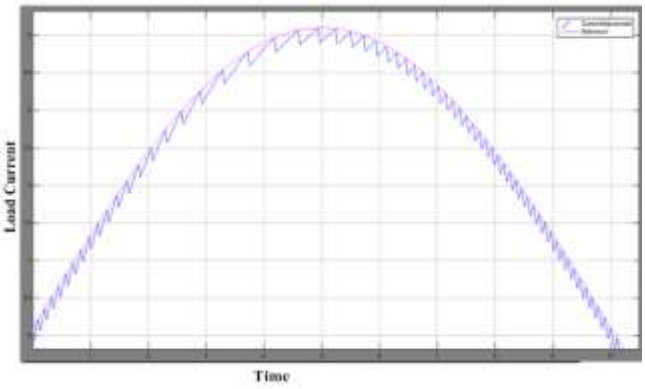

Figure 10 *Zoom in Inverter Output Current at f_{sd} = 1000KHz*

Now, for the THD analysis, the THD of the high sampling time system is more as compared to the low sampling time system as shown in Figure 11-13 respectively. This is due to the load current is cross the Hysteresis band boundary.

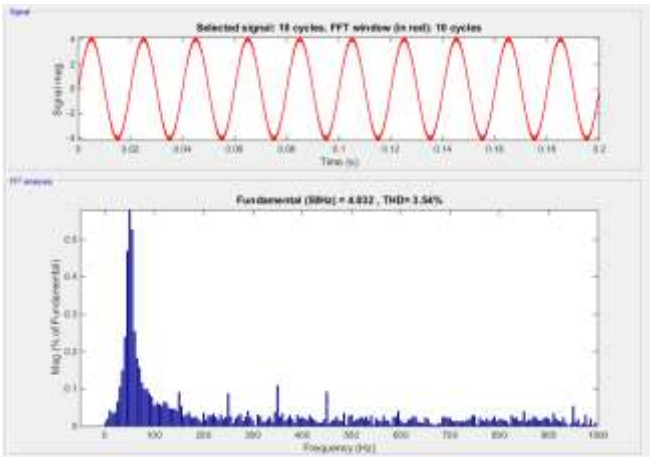

Figure 11 *Total Harmonic Distortion (THD) of the Inverter's Output Current at f_{sd}= 10KHz is 3.54%.*

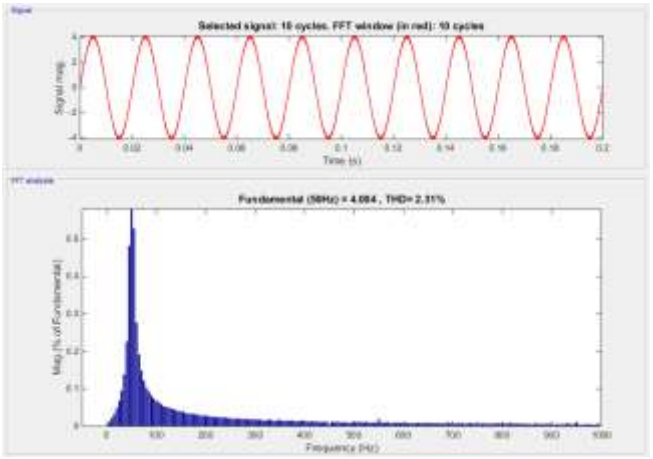

Figure 12 *Total Harmonic Distortion (THD) of the Inverter's Output Current atf_{sd} = 100KHz is 2.31%.*

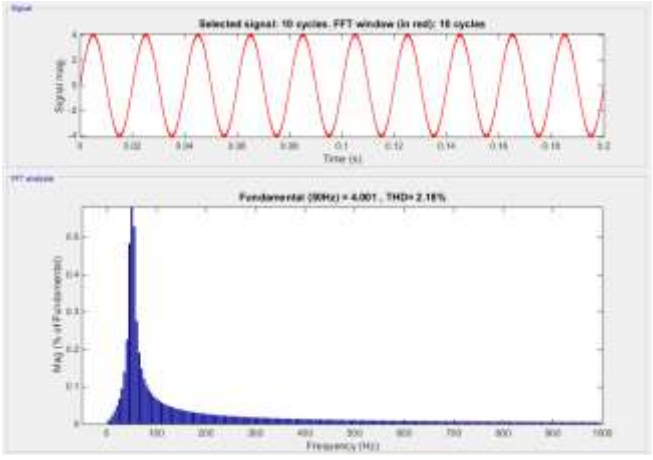

Figure 13 *Total Harmonic Distortion (THD) of the Inverter's Output Current at f_{sd} = 1000KHz is 2.18%.*

5. Conclusions

This research explores the non-periodicity in current tracking within a digitally implemented Hysteresis Current Controller (HCC) and examines how the sampling frequency influences its switching dynamics.The findings reveal that reducing the sampling time prevents overshoot; however, it also shortens the load current switching duration and lowers the instantaneous grid voltage amplitude. This can lead to a loss of control, causing the load current to exceed the hysteresis band. To address this issue, a fast-acting current controller is necessary, particularly in phases where switching time and grid voltage are higher. Additionally, when current overshoot occurs, the peak can reach up to twice the hysteresis band (2h), increasing current ripple beyond the allowable limit. The study further highlights that HCC is easy to implement when the grid voltage or back EMF is zero. However, maintaining stability under varying conditions requires precise tuning of the sampling frequency and an optimized control strategy. By refining these parameters, current ripple can be effectively minimized, ensuring stable and efficient operation of grid-connected systems and electrical drives. These insights contribute to improving the reliability and performance of digitally controlled HCC in practical applications.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
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- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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