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Research Article

A Digital Phase Locked Loop Design from analysis to implementation : application to FSK demodulation

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Abstract:

The study of Phase Locked Loops (PLL) has been heavily treated in literature and most of the theoretical and the analytical results of such are verified using simulations. Here we provide guidelines of a digital PLL design and his circuit implementation on Pspice simulator (16.6 version) for both analyzing and verifying the theoretical results. In fact, the digital PLL is a hybrid device where only the phase detector is built from a digital circuit and the remaining blocks are still analog ones.

1. Introduction

Phase-Locked Loops are a useful control system tools commonly used in communications, radar, sonar, control engineering, and many other applications. In communications, PLLs are used for carrier tracking, frequency synchronization, phase synchronization, and symbol timing synchronization. Each PLL system to be implemented presents an optimal solution for its design. For example [1], there are applications of PLL in communications where the system is used to extract the clock signal from a possibly noisy information signal. In such application, noise suppression is essential. Another different application is frequency synthesis. Here, the noise effect is not important, but the synthesizer must be able to switch quickly from one frequency to another, indicating the capture time as the principal parameter. Our DPLL design will articulate on eliminating superimposed noise within the input signal.Digital Phase-Locked Loops (DPLLs) are fundamental building blocks in modern electronic systems, providing robust solutions for frequency synthesis, clock recovery, and synchronization in applications ranging from wireless communications to power electronics and navigation systems. The transition from analog to digital PLLs has enabled greater integration, programmability, and resilience to process, voltage, and temperature variations [2-6]. DPLLs typically comprise digital phase detectors, loop filters, and digitally controlled oscillators, all of which can be implemented using standard digital design flows, FPGAs, or ASICs [4,7-9]. Recent research has focused on optimizing DPLL architectures for low jitter, fast locking, low power consumption, and adaptability to various application domains, including GPS synchronization [10], wireless communications [11,12], and grid-connected power systems [13]. Innovations such as sliding mode control [14], fuzzy logic filters [15], and automated design tools [16,17] have further enhanced DPLL performance and design efficiency. This review synthesizes the state-of-the-art in DPLL design, from theoretical analysis to practical implementation, highlighting key methodologies and performance trade-offs.

2. DPLL design and application

The figure 1 shows a mathematical model of the DPLL, which consists of three functional blocks: the Phase Detector, the Loop Filter, and the Voltage Controlled Oscillator. Here, the only truly digital

part is the Phase Detector as mentioned.In terms of principle working, the Phase Locked Loop is used to synchronize the output phase and frequency of the Controlled Oscillator to match the phase and frequency of an input signal [1].

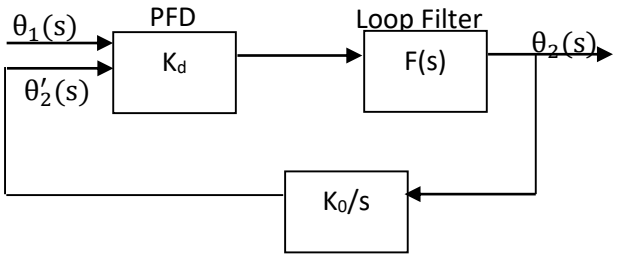

Figure 1. *DPLL functional block diagram*

2.1 The Phase Frequency Detector (PFD)

When the PLL is locked, a Phase Detector presents at its output a high-frequency component which is eliminated by the Loop Filter and a remained useful low-frequency component depending only on the error phase $\theta_e(t)$ at locking [25], is then:

$$u_d(t) = K_d sin\theta_e \qquad (1)$$

With K_d, the sensitivity or gain of the detector. The characteristic of such a Phase Detector is therefore sinusoidal [19], figure 2.

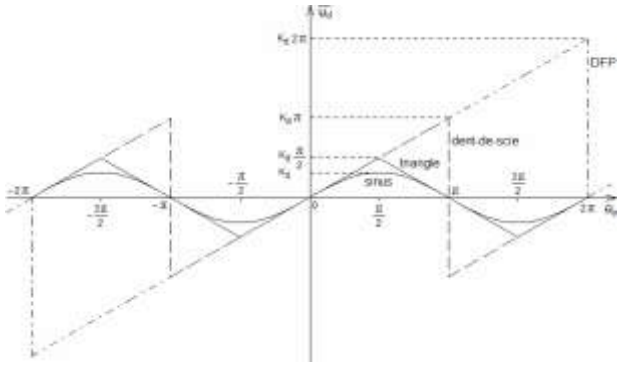

Figure 2*. Phase detector characteristics*

The phase comparator with charge pump or Phase-Frequency Detector (PFD) in figure 3 presents when the loop is not yet locked, a signal at its output which does not only depend on the phase error but also on the frequency error Δω. The PFD is designed from two D flip-flops whose outputs are denoted "UP" and "DN", respectively. By an additional AND gate removing the output state UP=DN=1 by acting on the CLEAR inputs of the two flip-flops, the PFD can be in one of the three remaining states (denoted -1, 0, 1) [10]:

UP=0, DN=1: state –1,
UP=0, DN=0: state 0,
UP=1, DN=0: state +1.

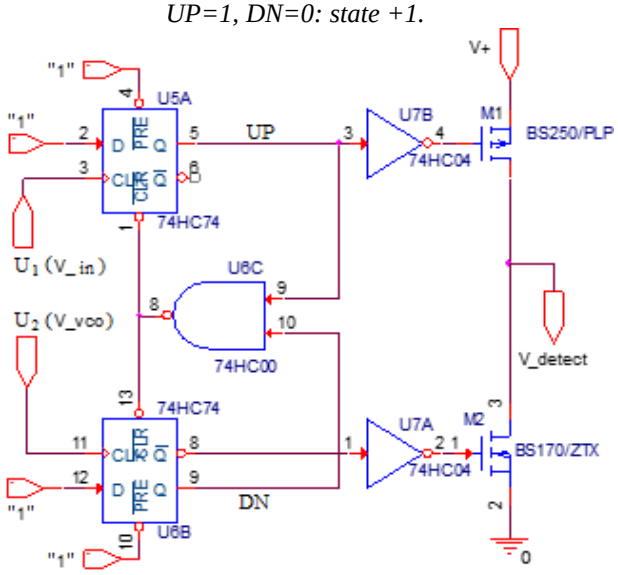

Figure 3. *Phase-Frequency Detector circuit*

The current state of the PFD is determined by the positive transitions of the input signals U_1 and U_2 as shown in the state diagram of figure 4 [1].Thus, a rising edge of U_1 forces the PFD to go to the next higher state, unless it is already at state +1. By analogy, a rising edge of U_2 forces the PFD to go to the next lower state, unless it is already in the -1 state.

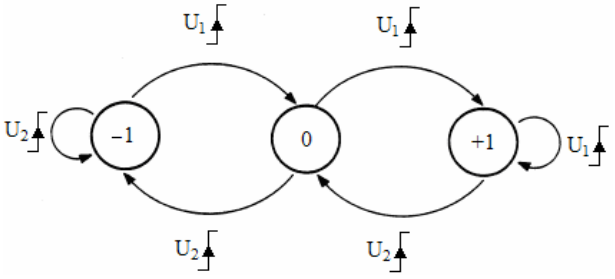

Figure 4. *PFD State Diagram*

The average output signal $\overline{U_d}$ is a logical function of the PFD state. When the PFD is at state +1, $\overline{U_d}$ must be positive, when the PFD is at state –1, $\overline{U_d}$ must be negative, and when the PFD is at state 0, $\overline{U_d}$ must be zero. This ternary signal can be interpreted as a logic signal with three states, where state $\overline{U_d} = 0$ corresponds to the high impedance state.The circuitry of figure 3 shows how the signal U_d is generated under a positive supply V_+. When the UP signal is high, the M_1 PMOS transistor saturates and U_d is equal to V_+. When the signal DN is high, the M_2 NMOS transistor saturates and U_d is zero. If the two signals are in the low state, the two transistors

are blocked and the output U_d floats since it is isolated by two high impedance state. Its theoretical value is $V_+/2$.The average voltage characteristic of U_d as a function of the PFD phase error has a sawtooth shape in figure 2, which extends between $\pm 2\pi$.When the phase error θ_e exceeds $+2\pi$, the PFD behaves as if the phase error has recycled towards zero, thus showing a characteristic curve periodicity of 2π. A similar reasoning can be made for phase errors smaller than -2π.In the $\pm 2\pi$ useful range, the average output voltage $\overline{U_d}$is proportional to the phase error θ_e.

$$\overline{U_d} = K_d \theta_e + \frac{V_+}{2} \qquad (2)$$

With a gain $K_d = V_+/4\pi$, which also represents the transfer function of the phase detector. The PFD being selected for our application, its gain under a 5V supply becomes $K_d = 0.4$ V/rd.The MOSFETs used in the PFD in figure 3 are chosen from those existing in the Pspice library: BS170/ZTX for the NMOS and BS250/PLP for the PMOS [10], which are both enrichment types.

2.2 The Loop Filter

In general, the phase comparator output contains undesirable terms often located in the upper part of the spectrum relative to the detection useful term. These useless components are filtered by the loop filter, which is necessarily a low-pass type. In order to lead to a second-order PLL, a first-order filter is required of which figure 5 gives the frequently encountered version [1,19,20].This filter is a passive lead-lag with one pole and one zero. A phase-leading or phase-advance action that comes from the zero is therefore combined with another phase-lagging or phase-delay action that comes from the pole of the filter transfer function. The filter transfer function is given by:

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s} \qquad (3)$$

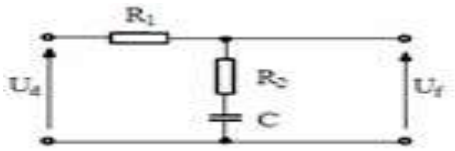

Figure 5. *Low-pass Loop Filter*

With time constants $\tau_1 = R_1C$ and $\tau_2 = R_2C$.

However, a special behavior of the loop filter manifests in the presence of the PFD detector type. This later does not ensure any current flow in the resistors R_1 and R_2 when it is in the high impedance state. Under this condition, the capacitor voltage remains theoretically unchanged. Neglecting leakage currents, the filter output signal U_f has a constant level when the PFD is in its 0 state. Thus, the filter acts as an ideal integrator, and its transfer function becomes [1]:

$$F(s) = \frac{1 + \tau_2 s}{(\tau_1 + \tau_2)s} \qquad (4)$$

The PFD with the passive filter combination, is often referred to as a charge pump. This means that at the high level of the PFD output signal, the charge flows into the filter capacitor in other words, the charge is pumped inside the capacitor. When the PFD output signal is at its low level, charge flows from the filter capacitor. That is to say, the charge is pumped out of the capacitor to ground. Pumping action stops, however, during state 0 of the PFD [22].In order to don't charge the passive filter output, an adaptation circuit in the first stage of the VCO is provided in figure 6. The filter signal is then amplified four times with a simple 741 operational amplifier followed by a follower as an adapter stage [26].

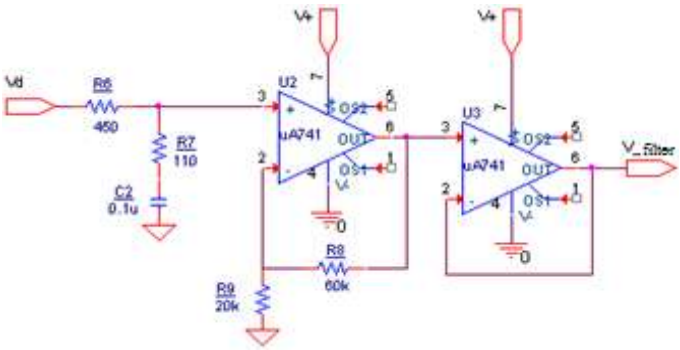

Figure 6. *Optimized Loop Filter circuit*

2.3 The Voltage Controlled Oscillator (VCO)

The VCO used in figure 1 oscillates at the angular frequency ω_2 which is determined by the loop filter output signal u_f :

$$\omega_2(t) = \omega_0 + K_0 u_f(t) \qquad (5)$$

Where ω_0 is the VCO center frequency and K_0 the VCO sensitivity or gain, in $(SV)^{-1}$.When the VCO

model uses the phase output θ_2 and not the frequency output ω_2, the VCO transfer function expressed by the Laplace Transform becomes:

$$\frac{\theta_2(s)}{u_f(s)} = \frac{K_0}{s} \qquad (6)$$

The VCO characteristic is to be determined from the central frequency ω_0 or the frequency range, which must be known. In most cases, the VCO is part of the DPLL integrated circuit. The datasheet indicates the range $u_{fmin} \leq u_f \leq u_{fmax}$ used for the control voltage (typically 1 to 4V for a 5V supply) [23]. The VCO sensitivity $K_0$is calculated as:

$$K_0 = \frac{\omega_{2max} - \omega_{2min}}{u_{fmax} - u_{fmin}} \qquad (7)$$

The VCO external components can also be determined, generally, by data-sheet indication, but our VCO is designed according to the circuit [20] in figure 7.

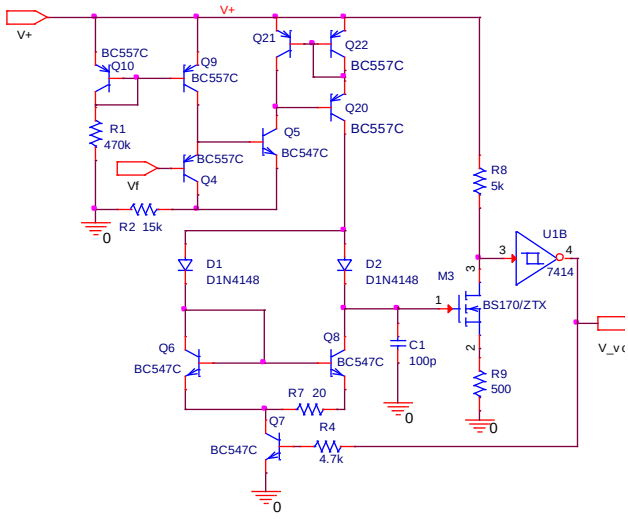

Figure 7. *Proposed VCO circuit*

The proposed VCO is a linear ramp relaxer based on a capacitor C_1 through which a charge-discharge current I flows. This current comes from a controlled voltage current source driven by the Loop Filter output V_f.The charge is accomplished through the fast diode D_2, and the rising ramp voltage at C_1 terminals is stopped once it reaches the first Schmitt Trigger threshold. The output V_{VCO} goes high and turns on the transistor Q_7 which has as an active load at its collector: a current mirror composed by transistors Q_6 and Q_8 becoming activated. The current circulation from the controlled source becomes now through transistor Q_6 and diode D_1, while the mirrored current by Q_8 and always equal to I, ensures the C_1 discharging. In this time, diode D_2 is blocked.The falling ramp voltage across C_1 is stopped when the second trigger threshold is reached. The output voltage V_{VCO} at the low level, inhibits the current mirror action and allows the charging current to flow again from the controlled source to C_1.

2.4 Working DPLL

The three DPLL circuit parts, in figures 3, 6, and 7, are assembled in a functional blocks into closed loop as shown in figure 8 [26].

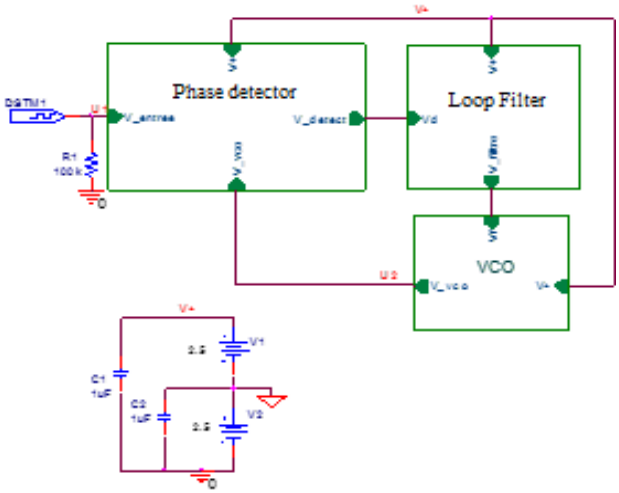

Figure 8. *DPLL Block diagram captured on Pspice*

When the DPLL is in the locked state, its performance can be analyzed by a linear model [2]. Considering the transfer function F(s) of the passive Loop Filter (equation 4), the DPLL transmittance H(s) has a second-order denominator that it is more convenient to put under normalized form, $s^2 + 2\varepsilon\omega_n s + \omega_n^2$ where ω_n represents the DPLL natural frequency, and ε, its damping factor. So we have:

$$H(s) = \frac{\omega_n^2(1 + \tau_2 s)}{s^2 + 2\varepsilon\omega_n s + \omega_n^2} \qquad (8)$$

Where:

$$\omega_n = \sqrt{\frac{K_0 K_d}{\tau_1 + \tau_2}} \quad and \quad \varepsilon = \frac{\omega_n}{2}\left(\frac{1}{K_0 K_d} + \tau_2\right) \qquad (9)$$

The damping factor ε has an important influence on the DPLL dynamic performance. For ε=1, the system is just damped. If ε is less than unity, the transient response of the DPLL becomes oscillatory.

The more ε decreases, the more the overshoot of the response increases. In most practical systems, the transfer function is optimal for$\varepsilon = 1/\sqrt{2}$ [23].

The bandwidth at −3dB becomes:

$$B = \omega_n\sqrt{-\lambda + \sqrt{\lambda^2 + 1}} \qquad (10)$$

Where:

$$\lambda = \frac{\omega_n}{K_0 K_d}\left(4\varepsilon - \frac{\omega_n}{K_0 K_d}\right) - 1 - 2\varepsilon^2 \quad (11)$$

2.5 DPLL application

In order to simulate the behavior of the designed DPLL in an angular demodulation operation, the hopping frequencies of an orthogonal FSK modulation are chosen first. Consider a sinusoidal carrier f_c = 200 kHz, modulated in FSK by random data of rate R_b = 2 kHz with an excursion ΔF = 15 kHz. The jump frequencies are therefore:

$$f_1 = f_c + \Delta F = 215\ KHz \qquad (12)$$

$$f_2 = f_c - \Delta F = 185\ KHz \qquad (13)$$

With modulation index h=ΔF/Rb = 7.5. The frequency band occupied by the FSK signal is:

$$B = 2(1 + h)R_b = 2(1 + 7.5)2\ KHz = 34\ KHz \quad (14)$$

The FSK transmitter follows the functional block diagram produced in Pspice according to figure 9, of which a certain number of logic circuits are associated with it. The generation of random binary data is ensured by the 74164 serial input and 8-bit parallel output shift register. Return branches are made from bits n=1 and m=6 through an XOR gate. The zero state at any output is avoided by setting an initial condition to 1 (HI).

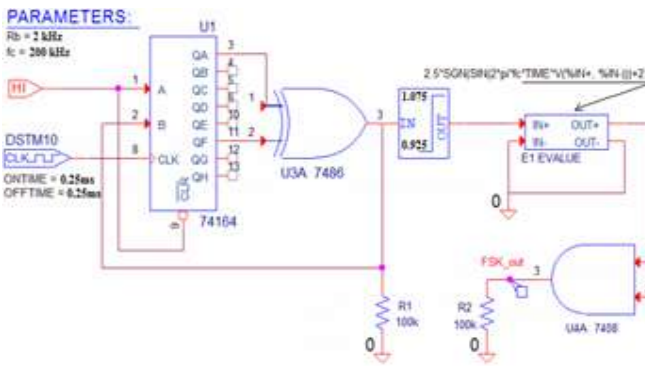

Figure 9. *FSK modulator*

3. Results and discussion

The VCO characteristic obtained in figure 10 is almost linear over the control range, V_f = 0.1V to 3.6V, for which the frequency varies from 50kHz to 967kHz (exceeding the decade by approximately one octave).The average slope of the characteristic is measured by the tangent at the midpoint of the curve (V_f = 1.8V, f = 585.6 kHz).That is, an average sensitivity of the VCO: $K_0 = 325\text{KHz/V} = 2.10^6$ rd/Vs.

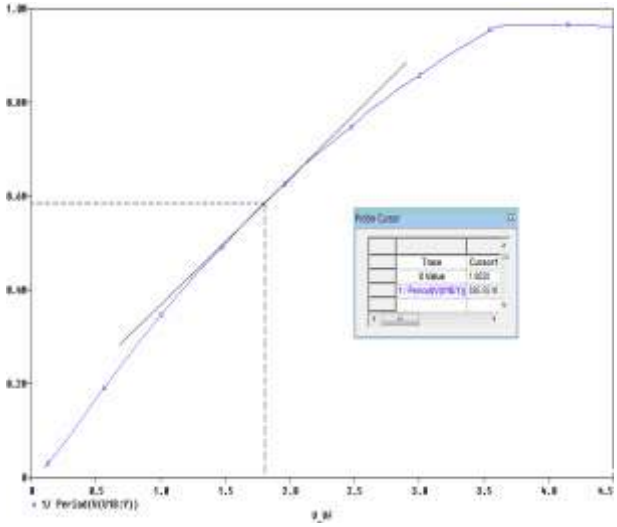

Figure 10. *Voltage-frequency characteristic of the VCO*

The Bode diagram relating to the Loop Filter with optimal time constants is drawn using System Vue tool [21], figure 11. A cutoff frequency at −3dB is measured equal to 2.95 KHz, practically identical to that found analytically:

$$f_c = \frac{1}{2\pi(\tau_1+\tau_2)} = \frac{1}{2\times 3.14\times(450+110)\times 0.1\times 10^{-3}} = 2.84\ KHz \qquad (15)$$

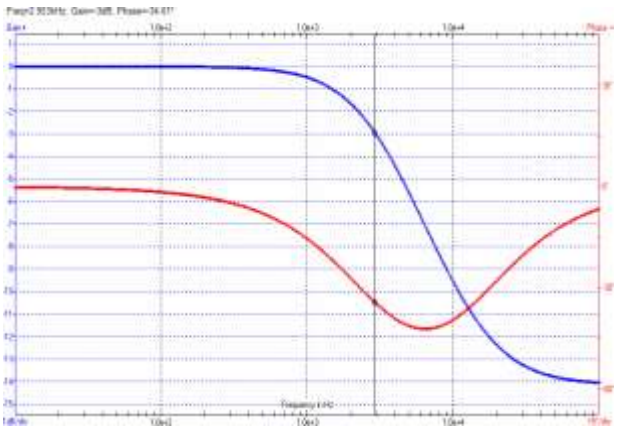

Figure 11*. Bode diagrams of the optimal Loop Filter*

The Bode diagram relative to the closed-loop DPLL system is also plotted using SystemVue [21], figure 12. The bandwidth at −3dB is estimated to be 35.9k Hz while that found analytically by using equations (10) and (11), is 35.25 kHz.

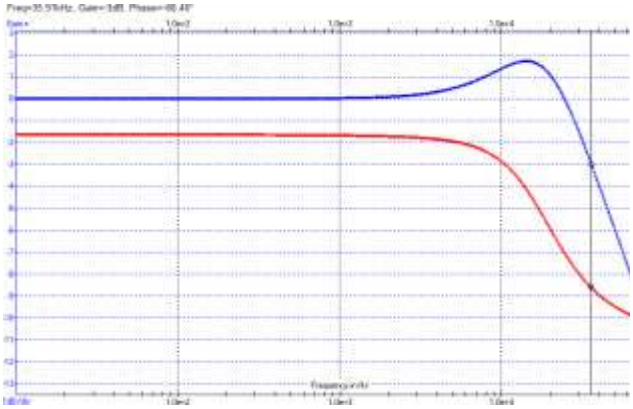

Figure 12. *Bode diagram of the closed-loop DPLL*

With the values assigned to the loop filter components, the designed DPLL offers its filter responses at input frequencies, 100kHz, 200kHz, and 625kHz.We notice there rectilinear shapes with little interference in the steady state of curves a and b, figure 13, while a BF waveform remains in the steady state of the filter response in curve.

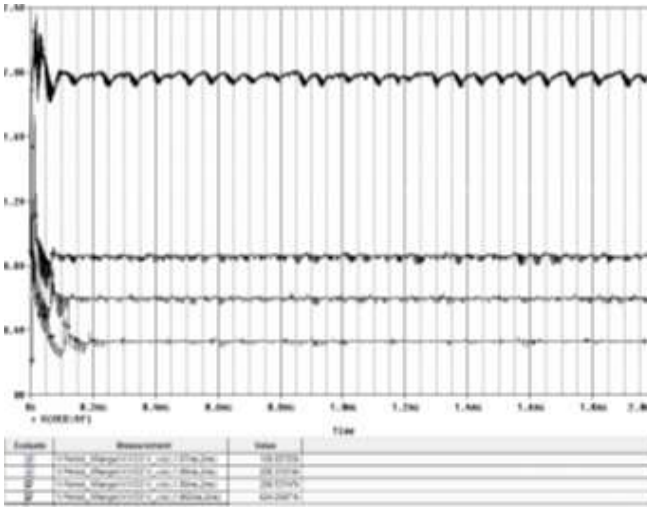

Figure 13. *Combined filter responses for four input frequencies*

In curve a, two filter voltage measurements corresponding to the 100 kHz input frequency, are taken at the beginning and at the end of the simulation: V_f= 851mV at t=0, and V_f = 331.567mV at t=2ms.The response time is about 0.2ms.In curve b, the two filter voltage measurements in response to the 200 kHz input frequency taken at the beginning and at the end of the simulation are: V_f = 851mV at t=0, and V_f = 604.5mV at t=2ms.The response time is about 0.12ms.Similarly in curve c, the filter voltage measurements in response to the 625 kHz input frequency corresponding to the simulation start and end are: V_f = 851mV at t=0, and V_f = 1.987V at t=2ms.The response time is difficult to measure, and it is between 0.1ms and 0.2ms.The zoom of the initial transient state in curve c is shown in figure 14. The waveform described as BF evolves at an average frequency equal to the natural frequency of the phase loop ($\omega_n/2\pi$ = 18.8 kHz), and constitutes the envelope of an HF parasite coming at the 625 kHz input frequency.

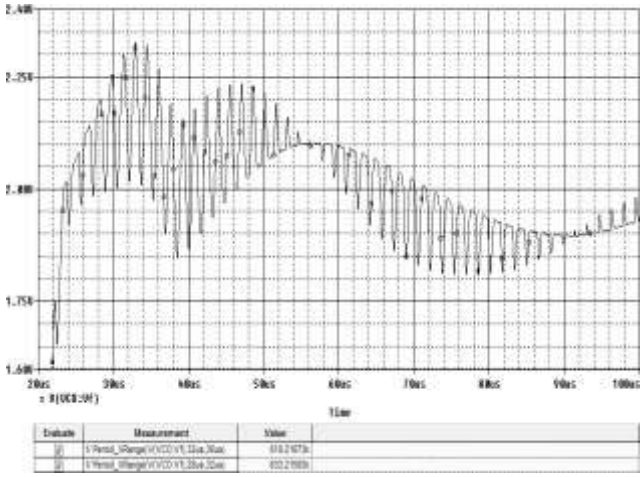

Figure 14. *Zoom of curve c in figure 12 showing an HF parasite at input frequency of 625 kHz*

All of the filter responses shown in curves a, b, and c have a common starting point, which is the bias filter voltage, V_f = 851mV. This biasing voltage at the loop filter output fixes a natural or proper frequency of the VCO, which is f_0 = 290.5 kHz measured on the voltage-frequency characteristic in figure 10.A fourth input at the natural frequency 290.5 kHz has been added. The corresponding filter response is plotted as curve d in figure 13, in which the measurements at the start and the end of the simulation are respectively: V_f = 183.736mV (may be disturbed by the initial phase difference with the input signal) and V_f = 857.143mV. The voltage of the filter reaches therefore its final value in practically 0.07ms, but remains in oscillation around it, at very low amplitudes not exceeding 59mV peak to peak.At the bottom of the figure 13, are gathered the frequencies reached by the VCO after 2ms of simulation in response to the four control voltages given by the loop filter. Small differences with 625 kHz, 290.5 kHz, 200 kHz, and 100 kHz input frequencies, are observed. This is because once the VCO frequency reaches the

input frequency value, the charge pump remains in its high impedance state under which the VCO capacitor C_1 cannot hold indefinitely its charge due to leaks. The voltage drops until it becomes perceptible by the Trigger, causing a new sufficient charge of C_1.The same cycle begins again, varying the VCO frequency in a small interval around the input frequency. The proper frequency of the VCO can be adjusted using an external DC voltage, added to the Loop Filter voltage by a non-inverting adder circuit in place of the follower in figure 6. A clock produced with the DSTM (figure 9) functional box makes it possible to clock the sequence of output bits, which is repeated after N clock pulses, thus fixing the maximum length of the sequence at N=2m−1=63 bits. The simulation duration being limited to 5ms, the number of bits of the random data also becomes limited to 10 bits following the bit rate fixed at 2kb/s. The modulating signal is the one presented in figure 15. The binary sequence evolves between levels very close to 1V, fixed by an amplitude limiter, figure 9. The 0.925V and 1.075V levels are necessary in order to fix the jump frequencies at 185 kHz and 215 kHz respectively. The discrete angular modulation is performed by the Evalue component, such that we have the frequency jump f1ou2 = fc×Vin = 200kHz×(0.925 or 1.075) = (185 or 215 kHz). A logic gate serves as a buffer. The FSK spectrum is given in figure 16.

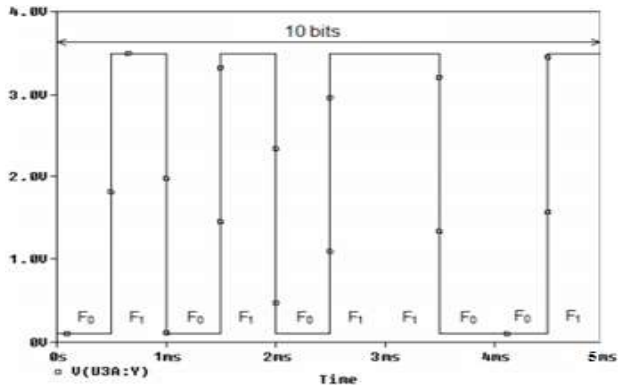

Figure 15. *Random data of modulating signal*

A necessary condition is to be fulfilled in order to satisfy good angular demodulation by PLL. The bandwidth of the PLL must contain the useful spectrum of the demodulated signal to be recovered. The bandwidth at −3dB of the DPLL being estimated to exceed 35 kHz, it is therefore considered to be quite sufficient to pass the demodulated BF information fixed at 2 kHz (main lobe of the Sinc) according to the bit rate adopted.

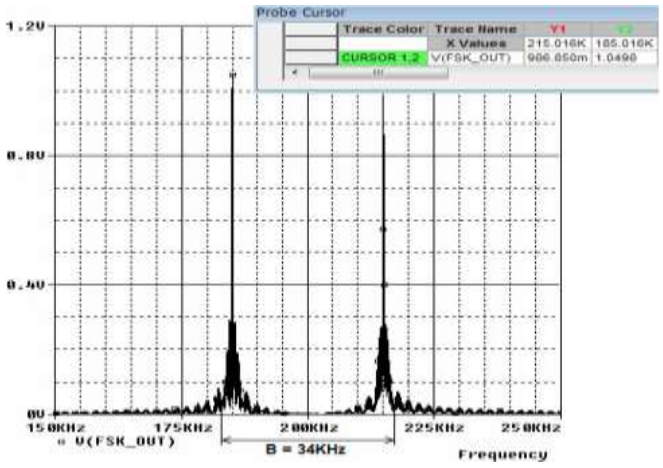

Figure 16. *FSK signal frequency spectrum*

The signal demodulated by the DPLL is represented in figure 17. The 1st bit is truncated by 0.15ms which represents the response time of the DPLL, due to the presence of the amplifier in its loop filter.

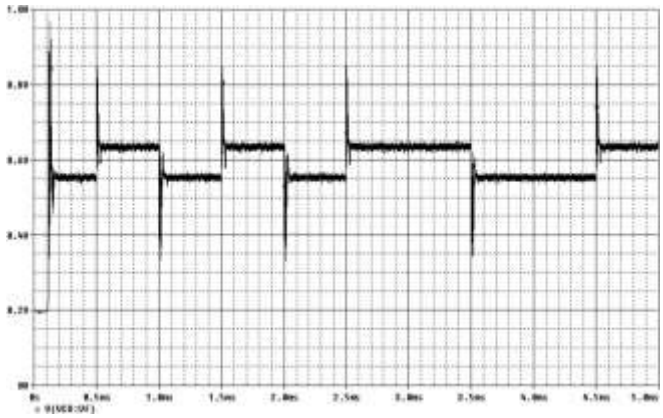

Figure 17. *Output demodulated by the DPLL*

The large peaks observed with each transition of the demodulated signal in figure 17 are linked to the very principle of operation of the DFP type phase detector used. This generates large pulses during each signal transition that coincides with an input frequency jump. The pulses are positive to catch up with the higher jump frequency or else negative to catch up with the lower jump frequency, figure 4. The current consumption is increased in these signal transition zones.

4. Conclusion

An assisted design by Pspice is used in order to achieve an optimized static and dynamic behavior of a DPLL. For this purpose, a phase-frequency detector type is chosen for its large action field of the

input phase, reaching up to ±2π.Optimum static precision of DPLL is achieved when associating the PFD detector with a simple 1st order passive filter, forming a charge pump in this case. The voltage-controlled oscillator part was the most difficult in design. On several occasions, it had to be improved in its voltage-frequency characteristic linearization. The second-order transmittance obtained for the closed-loop DPLL is assigned with an optimal damping factor of $1/\sqrt{2}$, thus reducing the DPLL response time to its minimum. The Pspice simulator remains the most accurate tool, because it takes into account the individual behavior of the electronic components realizing the DPLL. Thus, it provides stable and convergent responses at the Loop Filter output but remaining parasitized by the charge pump nonlinear operation. The filter is dimensioned by considering a set of components that responds to the optimality of the time constants of the loop filter. Satisfactory filtered signals were obtained as a result. An application in communications was the subject of our study on the behavioral aspect of a designed PLL. Thus, after choosing FSK modulation, the PLL demodulation application aims to recover the random sequence of information. For this, data files of the modulations envisaged are prepared using a simple modulator based on functional block diagrams under Pspice or by Matlab program.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
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- **Author contributions:** The authors declare that they have equal right on this paper.
- **Funding information:** The authors declare that there is no funding to be acknowledged.
- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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