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Research Article

Electrical Resistivity and Minority Carrier Lifetime Distribution in Directional Solidification of Silicon Ingot

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Abstract:

In this work, the main electrical wafer qualities were studied through resistivity and minority carrier lifetime variation, as a function of wafer position. The multi-crystalline silicon ingot was grown by directional solidification using the so-called -*Heat Exchanger Method* (*HEM*). The solid-liquid interface moves upwards from the bottom to top of the crucible. The growth rate is controlled so as to favour the growth of a high quality crystal structure by finely adjusting the position of the heat exchanger -*HEX* -block and the heater temperature value. The goal is to obtain vertically aligned grains which confirm a good directional growth. The achieved analyses were conducted by using the quasi-stationary photo conductance (QSSPC) and the four probe techniques. The ingot produced exhibits uniform large grain morphology with vertically-oriented grain boundaries. The resistivity for corner and center brick's present a maximum value of 2.3 Ω.cm and 1.69 Ω.cm respectively, after half (50%) of growth, and a minimal value in the first and final stages of solidification. In the beginning of growth, the initial minority carrier lifetime value is 3.23µs and 3.96µs for corner and center bricks respectively. Both lifetimes values grow to the maximum with 8.55µs and 14.05µs for corner and center bricks respectively, at the middle solidification position. The variation of electrical resistivity and minority carrier lifetime is probably affected by the impurity concentration, structural defects and grain structure.

1. Introduction

The Photovoltaic (PV) solar energy has been presented as an alternative source of electricity. More than 95% of commercial PV modules are made from crystalline silicon [1]. Despite the huge growth of monocrystalline silicon part, multi-crystalline silicon technology still exists in the cell market with the important share of silicon grown as ingots [2]. The directional solidification technique (DS) is the main method used to produce the multi-crystalline silicon (mc-Si) ingot with high quality wafer, in order to get high efficiency solar cells. The silicon wafer costs constitute a large part of the total cost (40%), thus several technologies have been competing for reducing cost production of silicon wafers. The Czochralski (CZ) technology is considered to be the first one to meet this goal. However, in terms of yield and productivity, CZ technology has the drawback of the energy consumption. Heat exchanger method (HEM) is the other strong technique for low-cost production [3].

The process control for the production of large multi-crystalline silicon ingot is more flexible than in CZ technology.

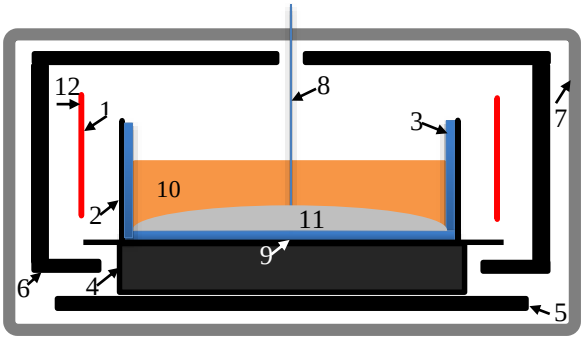
The quality of crystal grown by directional solidification is largely determined by the thermal field and growth rate, which directly affects both the yield of ingot process and the solar cell performance of resulting wafers [4] .

The mc-Si is an important material with the advantages of a low production cost and a relatively high conversion efficiency of solar cells. In this work, the DS process, used for production of multi-crystalline silicon ingots, take place in a HEM furnace manufactured by GT-Equipment Technologies Inc. producing 80 kg ingots in each run. The quality of resulting wafer was investigated thanks to resistivity and quasi-stationary photo conductance QSSPC techniques.

2. Material and Methods

2.1 Directional solidification process

In our work, the directional solidification process used for production of m-c silicon ingots, take place in a HEM furnace manufactured by GT-Equipment Technologies Inc. The configuration of the HEM furnace for growing mc-Si ingots is presented in Fig. 1.



1 Heater - 2 Graphite parts - 3 Crucible - 4 Heat exchanger bloc (Hex) - 5 Insulation - 6 Graphite insulation - 7 Furnace enclosure - 8 Quartz rods' - 9 Hex Thermocouple (T_{Hex}) - 10 Silicon melt-11 Solid silicon -12 Pyrometer

Figure 1. *HEM furnace schematic representation.*

In this production process, solar grade (SoG) silicon feedstock and doping element boron (in order to produce p-type materials with resistivity in the typical range of 0.8- 1.2 Ohm cm) were charged in the high purity silica crucible coated with silicon nitrate (Si_3N_4), the dimensions of the square crucible were 44x44x38 cm^3 with capacity of 80 kg of SoG silicon. This ingot supported with graphite plates is placed in a furnace. The pyrometer installed near the outer wall of the graphite resistance heater was used to control the heater power and monitor the temperature of the furnace during the whole process.

The furnace is provided also with thermocouples installed in the center of heat exchange bloc in order to get the temperature (of melt and solid silicon) measurements at this point (T_{Hex}).

The furnace chamber is evacuated to 0.01 torr, heat is applied by the graphite resistance heater until the charge is melted at 1560°C. After stabilization of the melted charge at the designed temperature (1440°C), the heat is extracted from the entire bottom of the crucible by the heat exchanger bloc system. The insulation and heat exchanger bloc gradually moved downwards by slowly speed, to reach 16 cm and 12 cm respectively. The solidification of silicon progresses from the bottom of the crucible to the top surface with the slightly convex solid-liquid interface [5]. In order to control the shape and velocity of the solid-liquid interface a movable silica rod is positioned in the center of the furnace, The growth rate of the ingot can be measured at regular intervals by probing the top ingot surface with a quartz rod. The rod is supported in the furnace coverlid in the center of the lid. The bottom of the rod is elevated above the top surface of the ingot.

The periodic measurement is performed by gently lowering the rod until it touches the top surface of the ingot, measuring the rod depth with a tape measure, then quickly raising the rod tip off the ingot surface. The measurements performed at regular intervals, once each hour, based on the time remaining; will result in excellent growth rate measurements. The furnace parameters: Hex temperature (T_{Hex}), the bottom insulation, heat exchange bloc, and interface position were controlled and adjusted for all directional solidification (DS) processes.

2.2 Slicing process

The multi-crystalline silicon ingot produce in HEM furnace sliced with diamond wire saw machine. The wire saws shape the ingots in to 16 squared blocks (bricks) with a cross section that is determined by the final wafer size witch 10x10 cm^2 (Fig. 2). The mc-Si blocks are cut off as scraps removing the top and bottom highly contaminated layer (1cm of each part) which tends to contain high amount of impurities (iron, aluminum, SiC, and Si_3N_4). The bricks were sliced by industrial multi wire saw machine (MWS) manufactured by HCT Wire Saw designed to slice mc- Si bricks into thin wafer. This machine used an abrasive liquid (slurry + Silicon Carbide SiC) carried by multi-wire web, this method used to slice silicon bricks into wafers with thickness of 320 µm.

2.3 Characterization

In this work, batch of selected wafers from center and corner position of silicon ingot are selected for investigation and characterization. Each sample for this investigation was chemically degreased with appropriate solvent in order to dissolve the machining fluids and other contaminants that might be on the wafer surface.

The resistivity of the wafers is determined by mean of four probe technique. The minority carrier lifetime was measured with the Quasi Stationary Photo Conductance QSSPC method using Siton instruments: WCT-120 Photo-conductance Lifetime Tester; the passivation of wafer surface was chemically performed using an iodine / methanol solution.

Figure 2. *Photograph of mc-Si ingot sliced in bricks.*

3. Results and Discussions

3.1 Process evaluation

As we can see from the data historic parameters saved and shown in Fig.3, in the first stage, the Hex temperature grows up form room temperature to the maximum temperature value of 1527.5°C where all silicon charge is melted. The next stage, before opening the insolation, the preparation growth steps was dropped the temperature of melted silicon to 1489.5°C in order to have a good control of growth velocity.

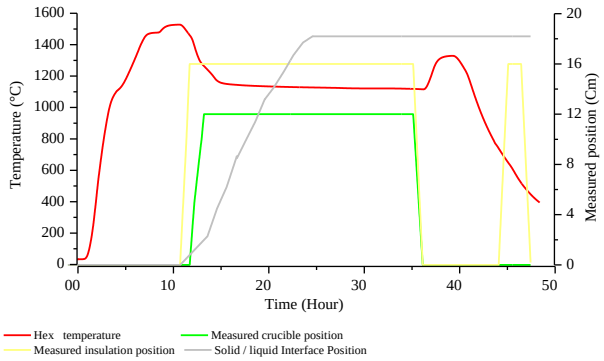


Figure 3: *Growth parameters of 80kg multi-crystalline silicon ingot and Solid-Liquid interface evolution*

The insulation reaches its final opening destination in 60 min with velocity of 0.27 cm/min, we observe a huge decreasing temperature from 1489.5°C to 1336.2°C. In the second step, the heat exchange bloc move down to his final position in 90 min with speed of 0.133 cm/min, the T_{Hex} temperature continues to decrease until reaching the value of 1206.6°C, this isolation and heat exchange bloc movement establish a temperature gradient between the top and the bottom of the silicon melt, which sets the growth (solid silicon) in motion.

At this stage, the grown portion reaches ~1.8 cm at the crucible bottom, this is probably due to super-cooling of silicon melt in this part of crucible.

The furnace temperature continues to be lowered, but much less aggressively, 3°C over ten hours and allows to the growth part get about 60% of the ingot height, in the center part. The second long step removes ~ 2°C, over nine hours and slows the growth rate to allow the corner grows without crack. In this our process, the ingot solidify at the center before the end of the growth process, this usually ensures a flat top and crack-free corners. This time allow the completed growth of corner and make sure that the silicon is solid before the temperature begins to fall. The temperatures were logged throughout the solidification process, which lasted approximately 15 hours for an average solidification velocity of 1.1 cm/h (3µm/s). Most impurities with segregation coefficient greater than 1 are segregated at the bottom of the mc- Si ingot, while impurities with segregation coefficient less than 1 are pushed to the top of the ingot [6]. The ingot growth is followed by decreasing the furnace temperature and reducing the temperature gradient. The stress (dislocations or stress cracks) produced inside of mc-Si ingot was annealed prior to cool down by holding ingot at fix temperature where dislocations and stress related defects can easily travel through the bulk of the lattice and be removed at natural boundaries or at the edges [7]. The final crystal structure is dominated by large columnar grains parallel to the solidification direction. The total duration of the process is around 48 hours.

3.2Electrical characterisation

The specific resistivity of wafers selected from corner and centre bricks, at different levels (according to the growth rate evolution), was investigated and presented in Fig.4. As we can observe from the Fig. 4, the corner brick resistivity vary from the initial value 1.18 Ω.cm to the final 0.92 Ω.cm, at 10% and 90% of growth rate respectively, with a high value 2.3 Ω.cm recorded at 50% of growth rate position of the brick. For the

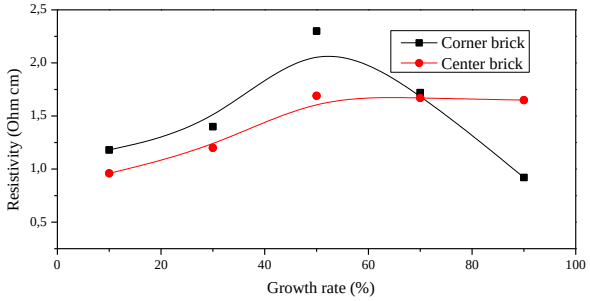


Figure 4. *Resistivity variation at different levels, for center (circle) and corner (square) bricks.*

center brick, the variation of resistivity is between 0.97 Ω.cm to 1.65 Ω.cm, respectively at 10% and 90% of growth rate, with a value of 1.67 Ω.cm in the middle part of solidification. The horizontal difference in resistivity between specimens taken from each growth rate position of center and corner bricks is very small; which results in a well-controlled geometry of the solid-liquid interface and well boron distribution according to the theory of directional solidification without mixing according to J. M. Kim et al [8], this fact implies that the solid / liquid interface remains flat during growth. The knowledge of resistivity, and subsequently doping concentration in silicon ingot, is very important in optimizing the manufacturing process.

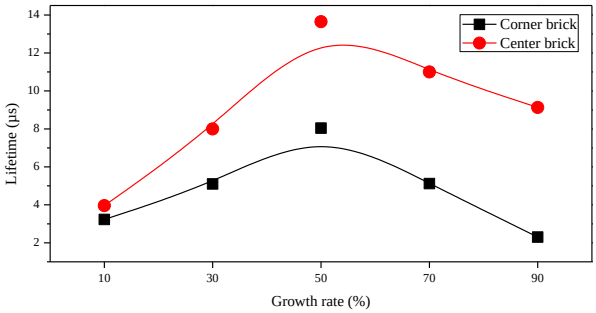


Figure 5. *Minority carrier lifetime variation for different heights in Si ingot*

Fig.5 displays the evolution of minority carrier lifetime in wafers taken from each part of bricks, as a graph, this will permit to see easily how the minority carrier lifetime value progress and to detect its changing according to the wafer position in brick and ingot, measured by QSSPC at $10^{15}cm^{-3}$ injection level.

The form and development of both graph evolution of corner and center brick are much closed. The initial low minority carriers lifetime value is 3.23µs and 3.96µs for the bottom (at 10% of growth rate) corner and center brick respectively, after this the both minority carriers lifetime value of corner and center grow to the maximum value (at 50% of solidification part), with 8.55µs and 14.05µs respectively, at 90% of growth rate the value of minority carriers lifetime decrees to 2.3µs for corner brick and 9.53µs for center brick.

This variation of minority carriers lifetime value, from the bottom to the top ingot, is due to directional solidification technique, where the heavy impurity segregate in the bottom part of ingot and the oxygen concentration decreases from the bottom to the top of the ingot [9] [10] [11].

However the minimum minority carrier lifetime is obtained at the bottom of the ingot. The minimum value of minority carrier lifetime present in top and corner bricks is due to the segregation of light impurity [6], and to the direct contact with the silica crucible.

4. Conclusions

In this study, we accomplished the growth of multi-crystalline silicon ingots by the HEM technique, then a subsequent brick and wafer characterization was realized. The obtained multi-crystalline silicon ingot presents a large grain size structure, with vertically oriented grain boundaries. The variation of resistivity and the minority carriers' lifetime investigation show different values according to position of wafer in the ingot.

The variation of electrical resistivity is probably affected by the impurity concentration and grain structure. The lifetime results are affected by the structural defects and grain morphology.

In a future work, different other techniques of characterization will be used to investigate more deeply the physical, chemical and electrical properties of the wafers, in order to understand the growth process, and to open the way for optimizing the wafer quality.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
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- **Data availability statement:** The data that support the findings of this study are available on

request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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