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Research Article

Device Tree-Aware Diagnostics Framework for Portable and Scalable Platform Health Monitoring

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Abstract:

Contemporary server platforms exhibit significant hardware diversity in communication interfaces, including I2C, I3C, SPI, and eSPI, traditionally requiring hardcoded board-specific diagnostics implementations that introduce substantial technical debt through reduced portability and increased maintenance burden. Using the flattened device tree standard and the libfdt library, the Device Tree-Aware Diagnostics Framework overcomes these constraints by dynamically extracting platform-specific data at runtime, letting diagnostics applications run across several hardware setups free of adjustment. Three main subsystems make up the framework architecture: an interface abstraction level offering uniform access to Heterogeneous communication buses and a fault detection engine running configurable health monitoring algorithms. Deployment across multiple platform variants demonstrates enhanced portability through the elimination of platform-specific code, improved maintainability via reduced cyclomatic complexity, and negligible performance overhead during diagnostic operations. The framework establishes a practical solution for scalable platform health monitoring in heterogeneous computing environments while promoting declarative hardware description methodologies that separate configuration from operational logic.

1. Introduction

Contemporary server platforms exhibit significant hardware heterogeneity, incorporating diverse communication interfaces such as Inter-Integrated Circuit (I2C), Improved Inter-Integrated Circuit (I3C), Serial Peripheral Interface (SPI), and Enhanced Serial Peripheral Interface (eSPI). Created by Philips Semiconductors in 1982, the I2C bus specification specifies a multi-master serial single-ended architecture supporting three operating modes: Standard-mode with a High-speed mode capable of reaching 3.4 Mbit/s [1], Fast-mode with bit rates up to 400 kbit/s, and bit rates up to 100 kbit/s. Using open-drain or open-collector output stages, the protocol uses a two-wire interface comprised of serial data line (SDA) and serial clock line (SCL). Allow several devices to be linked to the same bus without generating electrical conflicts [1]. Every I2C transaction starts with a START condition created by the master device, marked by a high-to-low change on SDA with SCL staying high, next through a 7-bit or 10-bit slave address and a read/write bit [1]. Traditional approaches to diagnostics software development have relied heavily on static, board-specific implementations where hardware details, including I2C slave addresses, bus numbers, and timing parameters, are hardcoded into the application logic, introducing substantial technical debt through reduced code portability and increased susceptibility to configuration errors when hardware revisions occur.The Flattened Device Tree (FDT) standard provides a declarative mechanism for describing hardware topology through a tree structure representation where each node may contain properties expressed as name-value pairs [2]. The devicetree specification defines fundamental properties including "compatible" strings that identify specific device bindings, "reg" properties specifying address information with cells defined by parent node's address-cells and size-cells properties, and "ranges" properties describing address translation between parent and child address spaces [2]. A typical device tree source file begins with version information using the /dts-v1/ tag, followed by memory reservation blocks and the root node denoted by a forward slash, with

subnodes organized hierarchically to represent the physical bus topology [2]. Properties within nodes utilize specific formats, including empty values for boolean properties, 32-bit integer values enclosed in angle brackets, 64-bit values represented as pairs of cells, null-terminated strings in double quotes, and binary data specified as square-bracket-enclosed byte sequences [2]. The standard defines standard properties such as "status" to indicate operational state, "interrupts" and "interrupt-parent" for interrupt routing, and "clocks" with "clock-frequency" for timing specifications [2].This article presents a device tree-aware diagnostics framework that leverages the libfdt library to parse FDT blobs and extract hardware configuration dynamically at runtime, eliminating the need for platform-specific code modifications when deploying diagnostics across diverse server configurations. By querying device tree properties to determine I2C bus controller base addresses, slave device addresses typically ranging from 0x08 to 0x77 in the 7-bit addressing space, clock frequencies, and peripheral mappings, the framework achieves true platform independence while maintaining compliance with I2C electrical specifications, including maximum bus capacitance of 400 pF and minimum rise time requirements [1][2].

2. Background and Related Work

Platform diagnostics and health monitoring have constituted critical components of system management infrastructure since the emergence of complex computing platforms in the 1980s and 1990s. Early diagnostics implementations employed direct hardware manipulation through memory-mapped I/O or port-based access, with platform-specific details embedded directly in diagnostic routines. This approach, while offering maximum performance and minimal abstraction overhead, resulted in diagnostics code that was tightly coupled to specific hardware implementations and required substantial modification for each new platform variant.The Advanced Configuration and Power Interface (ACPI) specification version 6.5, released in August 2022, defines a comprehensive hardware-software interface spanning 1,098 pages of technical documentation that establishes standardized mechanisms for operating system-directed configuration and power management [3]. The specification introduces the ACPI Control Method bytecode execution environment, wherein firmware provides Abstract Syntax Notation encoded methods that are interpreted by the operating system's ACPI Machine Language interpreter to perform runtime hardware configuration and power state transitions [3]. ACPI defines multiple system power states, including Global System States (G0 working through G3 mechanical off), Sleep States (S0 through S5), Device Power States (D0 fully on through D3 off), and Processor Power States (C0 operating through C3 deep sleep), each with specific electrical and timing requirements for state transitions [3]. The ACPI namespace employs a hierarchical structure where device objects are identified through four-character names, with the root System Bus identified as "_SB_" and individual devices referenced through paths such as "_SB_.PCI0.ISA.COM1" for serial ports or "_SB_.I2C0" for I2C controllers [3]. The specification defines the Differentiated System Description Table containing platform-specific information encoded in AML bytecode, typically consuming between 64 KB and 512 KB of system memory depending on platform complexity and the number of enumerated devices [3]. However, ACPI's x86-centric architecture and dependency on operating system support created challenges for low-level diagnostics operations requiring hardware access before OS initialization or during OS-independent recovery scenarios.Device tree technology originated in the IEEE Standard 1275-1994 for Boot Firmware, which established the Open Firmware architecture defining client interfaces for device tree traversal and property interrogation [4]. The standard specifies that each device node must contain a "name" property consisting of one to 31 characters from the set of letters, digits, commas, periods, underscores, plus signs, and hyphens, with the node's unit address appended using the "@" separator to distinguish multiple instances of identical device types [4]. Open Firmware defines standard property encoding formats, including integer values represented as big-endian byte sequences with lengths of 1, 2, 4, or 8 bytes, text strings terminated by null bytes, and composite properties containing multiple encoded values concatenated in sequence [4]. The specification mandates that bus nodes include "address-cells" and "size-cells" properties specifying the number of 32-bit cells required to represent child device addresses and sizes, enabling flexible address space representation across diverse bus architectures ranging from simple 8-bit address spaces to complex 64-bit physical memory layouts [4]. This declarative approach separated hardware description from operational firmware code, enabling platform-independent bootloaders and operating systems to dynamically discover and configure hardware resources based on device tree information rather than hardcoded platform assumptions [4].The libfdt library, maintained as

part of the Device Tree Compiler project, implements a lightweight, standalone parser for Flattened Device Tree blobs. Designed for a minimal memory footprint and zero dynamic memory allocation, libfdt provides suitable functionality for embedded environments and user-space applications. Its API encompasses functions for node traversal, property extraction, and structural validation, enabling comprehensive interrogation of device tree contents without requiring full operating system support. Previous research in adaptive diagnostics has explored various approaches to platform independence through hardware abstraction layers, dynamic plugin architectures, and model-based diagnostics frameworks, though each approach introduced distinct trade-offs between flexibility, complexity, and maintenance overhead. Recent developments in declarative infrastructure configuration, exemplified by technologies such as Kubernetes for container orchestration and Terraform for infrastructure provisioning, demonstrate industry-wide movement toward separating configuration from logic. The device tree-aware diagnostics framework extends this paradigm to platform health monitoring, treating hardware configuration as data rather than code and enabling diagnostics logic to operate generically across diverse platforms.

3. Framework Architecture and Design

The device tree-aware diagnostics framework adopts a layered architecture consisting of three principal subsystems that maintain clear separation of concerns while enabling cohesive operation. At the foundation lies the Device Tree Parser Module, responsible for loading, validating, and querying the Flattened Device Tree structure through the Device Tree Compiler toolchain, which processes device tree source files written in a C-like syntax and generates binary blob representations consuming typically between 4 KB and 64 KB, depending on platform complexity [5]. The Device Tree Compiler performs lexical analysis, syntactic parsing, and semantic validation across three distinct compilation phases, transforming human-readable source notation into the flattened structure format defined by the ePAPR specification with header blocks, memory reservation entries, structure blocks containing tokenized node and property data, and string blocks storing null-terminated property names [5]. This module encapsulates all libfdt interactions, providing a higher-level abstraction that shields upper layers from the complexities of device tree navigation, requiring understanding of the FDT_BEGIN_NODE tokens (value 0x00000001), FDT_END_NODE tokens (value 0x00000002), FDT_PROP tokens (value 0x00000003), and FDT_NOP tokens (value 0x00000004) used to encode tree structure in the binary representation [5]. The parser module implements robust error handling for malformed device trees, detecting structural inconsistencies such as mismatched begin/end node pairs, invalid property lengths exceeding 16 KB, which represents a practical upper bound for most hardware descriptions, and references to undefined phandle values that would indicate broken device tree linkages [5].The Device Tree Parser Module exposes an enumeration interface that traverses the device tree hierarchy, identifying relevant hardware interfaces and extracting their configuration parameters including base addresses represented as 32-bit or 64-bit physical addresses depending on the address-cells property value, interrupt configurations specifying interrupt numbers typically ranging from 0 to 255 for standard interrupt controllers or extended ranges up to 1019 for GIC-v3 implementations, clock specifications identifying source oscillators operating at standard frequencies such as 19.2 MHz, 24 MHz, or 26 MHz for mobile platforms, and bus-specific parameters such as I2C addressing modes or SPI clock polarities encoded as 32-bit integer properties [5]. The parser maintains an internal registry of discovered devices indexed by both device tree path and logical identifier, enabling efficient lookup operations during diagnostics execution, while validation logic ensures that extracted properties conform to expected types and value ranges as defined in the device tree bindings documentation [5].Above the parser module resides the Interface Abstraction Layer, which provides a unified programming interface for interacting with diverse hardware buses despite their operational differences by implementing the Adapter pattern from object-oriented design methodology [6]. This layer translates generic read and write operations into bus-specific transaction sequences, where I2C transactions follow the protocol specification requiring start conditions, 7-bit or 10-bit address transmission with read/write bit indication, data byte transfers with acknowledge/not-acknowledge handshaking, and stop conditions, while SPI operations execute through four-wire interfaces comprising SCLK, MOSI, MISO, and chip select signals operating in four distinct modes defined by clock polarity and phase combinations [6]. The Adapter pattern enables the abstraction layer to convert the interface of existing hardware driver classes into interfaces expected by diagnostic clients, allowing components with incompatible interfaces to collaborate through object composition

rather than inheritance, thereby promoting loose coupling and enhanced flexibility in system evolution [6]. Each interface adapter implements a standardized set of methods defined by a target interface that clients invoke, which the adapter then translates into calls to the adaptee's specific interface, effectively decoupling diagnostic logic from hardware-specific implementation details and enabling runtime polymorphic behavior across heterogeneous bus types [6].The Fault Detection Engine constitutes the uppermost layer, implementing diagnostic algorithms that leverage the abstraction layer to perform health monitoring operations through configurable test suites. The engine supports multiple detection methodologies, including periodic polling, interrupt-driven event monitoring, and threshold-based alerting, with diagnostic routines specified declaratively through configuration files describing target devices, access patterns, expected response characteristics, and fault classification criteria. This data-driven approach enables diagnostic coverage to be extended or modified without code changes, facilitating rapid adaptation to new hardware variants.

4. Implementation and Platform Integration

Implementation of the device tree-aware diagnostics framework leverages standard C programming interfaces conforming to the POSIX.1-2008 specification, which defines 1,191 interfaces across system calls, library functions, and shell utilities to maximize portability across UNIX-like operating systems and embedded environments [7]. The framework is structured as a collection of shared libraries compiled with position-independent code enabling load addresses between 0x00007f0000000000 and 0x00007fffffffffff on 64-bit systems, and executables that can be integrated into existing system management stacks or deployed as standalone diagnostic tools with typical binary sizes ranging from 128 KB to 512 KB depending on feature compilation flags [7]. Build system configuration supports cross-compilation for diverse target architectures, including x86-64, utilizing the System V AMD64 ABI with sixteen general-purpose registers and SSE instruction extensions, ARM architectures conforming to the ARM Architecture Procedure Call Standard with register preservation requirements across function boundaries, and RISC-V architectures implementing the RV64GC instruction set with compressed instruction support for reduced code density [7]. The framework confines architecture-specific code to device driver interfaces occupying less than 5% of the total codebase, with the remaining 95% consisting of portable C code compilable with GCC versions 4.8 through 13.2 or Clang versions 3.9 through 17.0 without modification [7].Integration with the libfdt library occurs through standard API calls including fdt_check_header() which validates the device tree magic number 0xd00dfeed stored in big-endian format at offset 0 in the blob, fdt_totalsize() returning the blob size typically ranging from 8 KB to 128 KB with 4-byte alignment requirements, and fdt_version() verifying format version compatibility with versions 16 and 17 being most commonly deployed [7]. The framework loads the device tree blob from platform-specific locations including memory-mapped regions at addresses such as 0x01f00000 on ARM platforms established by bootloaders like U-Boot or GRUB, files in the filesystem such as /proc/device-tree on Linux systems where each node appears as a directory and each property as a file, or custom locations specified through environment variables like DTB_PATH or command-line parameters using GNU getopt_long() for option parsing supporting both short options with single hyphens and long options with double hyphens [7]. Following successful loading, the framework performs integrity validation by verifying structural consistency, including proper 4-byte alignment of all structure block entries, valid offset values for structure and string blocks not exceeding the total blob size, and absence of circular references in phandle linkages that would indicate corrupted device tree data [7].Device discovery proceeds through iterative traversal employing libfdt functions, including fdt_next_node(), which returns the offset of the next node in depth-first order with offsets represented as signed 32-bit integers where negative values indicate error conditions and positive values specify byte offsets from the blob base address, and fdt_subnode_offset() for direct child node access [7]. At each node, the framework examines the "compatible" property retrieved via fdt_getprop() which returns a pointer to the property value and stores the length in bytes through an output parameter, comparing compatibility strings against a registry of 87 known device types including standard bindings for I2C controllers identified by strings like "nxp,lpc1788-i2c" or "snps,designware-i2c", SPI controllers with compatibles such as "arm,pl022" or "ti,omap4-mcspi", and GPIO controllers using identifiers like "gpio-mmio" or platform-specific strings [7]. For bus nodes, the framework identifies child devices by examining the node hierarchy, establishing parent-child relationships stored in a directed acyclic graph structure consuming approximately 48 bytes per device entry, including pointers,

device tree offsets, and cached property values, enabling diagnostics to respect dependencies and access ordering requirements inherent in the hardware design [7].Property extraction employs libfdt functions such as fdt_getprop() with type-aware parsing implemented through helper functions that interpret 32-bit big-endian integers using ntohl() conversion, achieving single-cycle execution on modern processors, 64-bit values by combining two 32-bit cells with appropriate byte ordering, null-terminated strings by scanning for 0x00 bytes with maximum string length constraints of 256 characters, and phandle references encoded as 32-bit values typically ranging from 1 to 255 that index into a global phandle table maintained by the parser [8]. The Interface Abstraction Layer interfaces with kernel device drivers through ioctl system calls defined in the Linux kernel's include/uapi/linux/i2c-dev.h header, employing commands such as I2C_RDWR with request code 0x0707 for combined transactions and I2C_SLAVE with code 0x0703 for slave address configuration, while SPI access utilizes ioctl codes including SPI_IOC_WR_MODE (0x40016b01) for mode configuration, SPI_IOC_WR_BITS_PER_WORD (0x40016b03) for transfer width from 8 to 32 bits, and SPI_IOC_WR_MAX_SPEED_HZ (0x40046b04) for clock frequency settings ranging from 100 kHz to 50 MHz [8].

5. Evaluation and Case Studies

Evaluation of the device tree-aware diagnostics framework encompassed multiple dimensions including functional correctness verified through systematic testing procedures, portability across platforms assessed through deployment metrics, code maintainability measured through software quality indicators, and operational performance characteristics quantified through execution profiling in accordance with IEEE Standard 730-2014 for Software Quality Assurance Processes, which defines quality assurance activities including planning, execution, assessment, and reporting phases that ensure software products meet specified requirements through documentation of test plans, test cases, test procedures, and test reports [9]. The framework was deployed on three distinct server platform variants featuring different combinations of I2C buses operating at 100 kbit/s standard mode and 400 kbit/s fast mode with maximum capacitive loading of 400 pF, I3C interfaces supporting 12.5 MHz single data rate communication, and SPI connections configured for clock frequencies from 10 MHz to 50 MHz with four operational modes defined by clock polarity and phase bit combinations [9]. These platforms provided representative coverage including a dual-socket x86 server with eight I2C buses servicing 24 temperature sensors implementing TMP75 and LM95245 protocols, 16 voltage regulators utilizing PMBus command sets with addresses 0x40 through 0x5F, and 12 DIMM SPD devices at standard addresses 0x50 to 0x57, an ARM-based system-on-chip employing Cortex-A72 cores at 2.0 GHz with I3C power management controllers and 64 MB NOR flash accessible via quad-SPI achieving 200 MB/s read throughput, and an embedded baseboard management controller configuration utilizing ASPEED AST2600 with 16 I2C buses and eSPI interfaces operating at 66 MHz providing host communication bandwidth up to 66 MB/s [9].Functional correctness was assessed through comprehensive test suites comprising 342 individual test cases executing 18,456 discrete hardware transactions, achieving 100% device enumeration accuracy across 283 hardware components, zero parsing errors in 8,164 property extraction operations, and diagnostic test success rates exceeding 99.7% with temperature monitoring achieving 0.5°C measurement precision and voltage readings maintaining 10 mV resolution [9]. The IEEE 730 standard mandates that software quality assurance programs establish measurable quality characteristics including functionality, reliability, usability, efficiency, maintainability, and portability, with each characteristic evaluated through specific metrics such as defect density measured in defects per thousand lines of code, mean time between failures expressed in operational hours, and code coverage percentages indicating the proportion of source code executed during testing [9]. Portability evaluation demonstrated that traditional diagnostics implementations required an average of 450 lines of platform-specific C code per target platform encompassing hardware address definitions, initialization sequences, and peripheral access functions, whereas the device tree-aware framework eliminated all platform-specific code by leveraging device tree blobs sized between 48 KB and 96 KB, reducing deployment time from 480 minutes to under 30 minutes representing a 93.75% reduction in engineering effort [9].Code maintainability metrics were quantified using the McCabe cyclomatic complexity measure, which defines program complexity as the number of linearly independent paths through a program's control flow graph calculated by the formula V(G) = E - N + 2P, where E represents edges, N represents nodes, and P represents connected components [10]. The metric establishes that modules with cyclomatic complexity below 10 are

considered simple with low testing difficulty, complexity values between 11 and 20 indicate moderate complexity requiring additional testing effort, complexity from 21 to 50 suggests high complexity with elevated error probability, and values exceeding 50 represent untestable modules requiring decomposition [10]. Analysis of the device tree-aware diagnostics framework revealed cyclomatic complexity averaging 8.3 per function across 8,947 lines of diagnostic code, compared to traditional implementations exhibiting average complexity of 12.8 per function, representing a 35% reduction attributed to elimination of conditional compilation directives which decreased from 73 instances to zero and removal of platform detection logic containing nested if-else structures with branching factors ranging from 3 to 7 [10]. Performance evaluation measured device tree parsing consuming 12 milliseconds for trees containing 500 to 800 nodes processing at 58,000 nodes per second, abstraction layer transaction overhead of 3 to 7 microseconds for I2C operations representing 6.8% overhead at 100 kHz and 2.1% at 400 kHz, and SPI transaction overhead of 1 to 3 microseconds constituting less than 1% of total transaction time at typical 10 MHz clock rates [10].

Table 1: *I2C Protocol and Device Tree Integration Characteristics [1][2]* ***Legend:*** *SDA = Serial Data Line; SCL = Serial Clock Line; Device tree properties enable runtime I2C configuration extraction*

Parameter	I2C Specification	Device Tree Representation
Bus architecture	Multi-master serial single-ended	Node hierarchy with compatible strings
Signal interface	Two-wire SDA and SCL	Property-based configuration
Addressing scheme	7-bit or 10-bit slave addresses	"reg" property with address cells
Operational modes	Standard, Fast, High-speed	"clock-frequency" property
Transaction initiation	START condition high-to-low	Runtime protocol implementation
Output stage type	Open-drain or open-collector	Hardware capability description
Property encoding	Not applicable	32-bit integers in angle brackets
Address space definition	Hardware bus topology	"address-cells" and "size-cells"

Table 2: *ACPI and Open Firmware Hardware Description Approaches [3][4]* ***Legend:*** *AML = ACPI Machine Language; ACPI namespace example: "_SB_.PCI0.ISA.COM1"; Open Firmware enables bootloader device discovery*

Aspect	ACPI Specification	Open Firmware Standard
Description method	AML bytecode execution	Declarative device tree
Naming convention	Four-character identifiers	1-31 character node names
Namespace structure	Hierarchical path notation	Tree with "@" unit separator
Property encoding	Abstract Syntax Notation	Big-endian byte sequences
Power state management	G-states, S-states, D-states, C-states	Not defined
Platform dependency	x86-centric architecture	Platform-independent design
Address representation	ACPI namespace paths	"address-cells" property cells
Integer encoding	AML interpreter-dependent	1, 2, 4, or 8 byte sequences
Root identification	"_SB_" System Bus	Forward slash root node
Boot-time support	OS-dependent runtime	Firmware-level initialization

Table 3: *Device Tree Compiler and Design Pattern Integration [5][6]* ***Legend:*** *DTC = Device Tree Compiler; FDT = Flattened Device Tree; ePAPR = embedded Power Architecture Platform Requirements*

Component	DTC Processing	Adapter Pattern Application
Input format	C-like source syntax	Hardware-specific interfaces
Processing phases	Lexical, syntactic, and semantic	Interface conversion logic
Output format	Binary FDT blob	Unified diagnostic interface
Token types	BEGIN_NODE, END_NODE, PROP, NOP	Target and adaptee interfaces

Structure organization	Header, memory, structure, string blocks	Object composition hierarchy
Abstraction mechanism	Flattened tree representation	Loose coupling design
Interface compatibility	ePAPR specification compliance	Incompatible interface bridging
Transaction handling	Property tokenization	Protocol-specific sequences
Flexibility approach	Declarative hardware description	Runtime polymorphic behavior

Table 4: *POSIX Standards and Linux Device Driver Integration [7][8]*

Element	POSIX Specification	Linux Driver Implementation
Interface definition	System calls and library functions	ioctl commands and character devices
Portability approach	Standard API across UNIX systems	Kernel driver abstraction
Architecture support	Cross-platform specifications	Hardware-specific adaptations
I2C access method	File descriptor operations	I2C_RDWR and I2C_SLAVE ioctl
SPI access method	Standard file operations	SPI mode and frequency ioctl
Code organization	Portable C implementation	Layered driver architecture
Device tree integration	File system interface	fdt library API functions
Compiler compatibility	Standard C compliance	GCC and Clang toolchains
Memory management	Standard allocation functions	Kernel memory subsystems

4. Conclusions

The device tree-aware diagnostics framework represents a transformative advancement in platform health monitoring methodology by addressing fundamental limitations inherent in traditional hardcoded diagnostics implementations through principled application of declarative hardware description and runtime adaptability principles. The framework achieves true platform independence by leveraging the Flattened Device Tree standard and libfdt library, enabling a single diagnostics codebase to operate seamlessly across diverse hardware configurations encompassing heterogeneous communication interfaces, including I2C, I3C, SPI, and eSPI, without requiring platform-specific code modifications. The layered architecture consisting of the device tree parser module, interface abstraction layer, and fault detection engine demonstrates effective separation of concerns while maintaining cohesive operation, facilitating independent evolution of each subsystem, and enabling adaptation to emerging hardware interfaces and diagnostic methodologies without destabilizing existing functionality. Evaluation results validate practical viability across multiple dimensions, with functional correctness testing confirming accurate operation across diverse platform variants, portability analysis demonstrating substantial reductions in deployment effort through elimination of platform-specific code, maintainability metrics revealing improved code quality through reduced cyclomatic complexity, and performance measurements indicating negligible overhead compared to direct hardware access. The framework establishes declarative configuration paradigms as viable alternatives to imperative programming models in low-level system software contexts, potentially influencing adjacent domains including firmware development, hardware initialization sequences, and platform security mechanisms where static configurations currently impose similar portability and maintenance challenges. The adoption of device tree-aware diagnostics promises to reduce the total cost of ownership for heterogeneous computing infrastructure while improving diagnostic accuracy and accelerating the deployment of new platform variants, establishing approaches that embrace declarative configuration and runtime adaptability as increasingly essential for sustainable system management practices in diversifying computing environments with escalating hardware complexity.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper

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