International Journal of Computational and Experimental Science and ENgineering (IJCESEN)

Vol. 11-No.4 (2025) pp. 9717-9725
http://www.ijcesen.com

ISSN: 2149-9144

Research Article

Design and Comprehensive Analysis of FinFET Spacers for Advanced Semiconductor Devices

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Article Info:

DOI: 10.22399/ijcesen.4477
Received : 15 September 2025
Revised : 25 November 2025
Accepted : 30 November 2025

Keywords

finFET,
Spacer,
Single k,
Dual k,
Sub threshold Swing

Abstract:

In modern semiconductor technology era focus more on performance improvement and reduction in size while realizing advanced applications using FinFETs (Fin Field-Effect Transistors). In this implementation process Spacers plays a crucial role for maintaining the proper energy efficiency to improve the performance. The main objective of this study investigates the impact of the spacer width and height dimension on the driving current, subthreshold slope (SS) and leakage current offered by the FinFET.The variability in FinFET performance caused by changes in spacer settings and process circumstances is evaluated using statistical analysis. In this study the comparative analysis between Single K and Dual K spacer techniques concentrates on Process variations and sub-threshold swing with different spacer materials. A variety of advanced modelling techniques are used to quantify and analyse the influences in order to maintain a trade-off in the spacer design. During the implementation process, it was found that when hafnium (HfO2) and nitride were combined, the underlap length of 2 nm produced improved electrical features with reduced drain induced barrier lowering (DIBL) up to 40 mV/V, whereas in air space, the DIBL was found to be 84 mV/V. When compared to single K dielectrics, dual K dielectrics improve subthreshold swing by attaining 75–78 mV/dec. An essential component of improved FinFET-based applications is spacer engineering. Performance measures such as DIBL, SS, and variability are impacted by material selection, dimensional tuning, and gate-stack design spacer settings. This study offers a framework for the development of future-generation FinFET-based device.

1. Introduction

In new era of deep submicron technology Fin-FET (Fin Field Effect Transistor) plays a key role in miniaturized device applications [1-3].The primitive components used for device applications focused more on power consumption and integration capability to meet the device performance. This research focus more on spacers technology based Fin-FET devices. [4-6].In Semiconductor design environment the performance analysis of FinFETs using spacers plays a crucial role. The primary objective of this research paper concentrates on semiconductor devices based on spacer technology via nano scale regime [7-9]. The spacer contains a thin dielectric material and the existence of the spacers in FinFETs lies in between gate electrode and channel of the semiconducting device. The spacers can change the device threshold voltage, subthreshold slop, leakage current, and overall performance efficiency [10-12]. It is necessary to focus more deeply on the balance between the features. The goal of this study is to further the ongoing pursuit of semiconductor excellence in this field. Knowledge of spacer design is crucial for next-generation semiconductor design and aids semiconductor engineers in improving design applications to get around design limitations and boost performance. The comprehensive

examination, comparisons, and advancements of spacer technology used in semiconductor-based devices are the primary topics of this research paper. Flat MOSFET efficacy is dramatically reduced by ongoing scalability at the sub-14 nm level, leading to higher current leaks and off-state power, both of which are crucial design criteria for next-generation CMOS [13-15]. The basis for the major achievements in the sector include the creation of new high-k/metal gate stacks, complex S/D technologies, mobility improvement technologies, and advanced multigate structures. The creation of improved multigate transistor designs through device simulation and the use of new manufacturing methods will be the main emphasis of this paper. The length of time needed to charge and discharge the load capacitance is significantly lengthened by the higher ON current. As a result, scaling increases integrated circuit speed while concurrently reducing parasitic presence in the transistors.

2. Literature Survey

Ludwig et.al presents an overview of fin-FET technology and its significance in advanced semiconductor devices [19]. M.R. Tripathy, A.K. Singh, and colleagues [20] compared the performance of all-silicon heterojunction TFET, In0.53Ga0.47As/Si heterojunction TFET, and GaSb/Si heterojunction TFET in their research. Small band gap materials should be employed at the source of the heterojunction in order to promote tunnelling at the heterojunction. Because Al2O3 has a higher dielectric constant than SiO2, it was used as the gate oxide in order to boost the ON current. This allowed the ON current to be increased. When using GaSb or In0.53Ga0.47As with SI, mismatches in the lattice and thermal co-efficients can result in heterojunction faults in the device. There has been research into both the DC and RF performance of the system. With lower saturation voltages (less than 40mV per decade) and higher IOFF: ION ratios, III-V/Si TFETs have been proven to be superior to other types of transistors.The SELBOX was used in conjunction with the heterojunction (HJ) partial ground plane PGP (TFET) to increase the IOFF/ION current ratio of the PGP transistor [21]. Throughout this article, Ge is cited as the major source of information. A device's DC attributes like as transfer characteristics, threshold voltage, and subthreshold swing (SS)are affected by its temperature. It was discovered that the biggest tunnelling current was $3.2x10^6$ V/m, which was the result of the highest electrical field. With the use of PGP, it is possible to increase the performance of SOI devices. The parasitic capacitances and cut-off frequency characteristics of the PGP SELBOX TFET have been measured and compared to those of other TFET devices to determine their RF performance. According to the findings of this investigation, there is relatively little effect of temperature on the performance of the proposed PGP SELBOX and SOI TFET devices in terms of power consumption. Z Wei and his colleagues [22] have developed an InAs/Si-based tunnel FET in order to reduce the short channel effects of the transistor. It was decided to use an analytical potential model with a channel length of 50 nm in order to model the drain current. Tarek Amen, Hasemeddin, and others [23] have proposed nitride heterostructures as a way to boost the ON current in a transistor. A piezoelectric polarisation field is generated in a nitride heterojunction as a result of the mismatch in the lattice structure. As a result, the ON current is increased. The subthreshold features of the heterojunction interface, on the other hand, are reduced by hot charge carriers that are created thermally. In order to mitigate this effect, an alloy-designed nitride TFET may be the best choice for your application.According to Venkatesh et al [24], analytical modelling of biosensors based on double-gate metal oxide semiconductor field effect transistors is possible. It is used in this case to determine the precise concentration of biomolecules. The structure and operating principle of the device are depicted in this model. The surface potential, threshold voltage, and sensitivity of the device, among other things, are all monitored throughout this process. Recent publication on source - drain engineering by A. Velso and team recorded that the nano sheet field effect transistors' performance can be enhanced by moving the wiring to back sideof the structure. This can also increase the scalability of the FET. Furthermore, few papers explore advanced spacer patterning techniques to enhance the performance and reduce variability in fin-FETs and various design patterns and structures were also studied [25-31].

3. Design Methodology

Using T-CAD, the FinFET was designed. The gate length (l) of the FinFET design depicted in Figure 1 is 10 nm, whereas the gate oxide thickness height (t) is 1 nm. The gate oxide thickness height "th" is 10 nm, and the spacing oxide low is 1 nm. There is a 5 nm gap oxide height.

The finFET design process ensures that spacer materials may be arranged and examined sequentially. The interior layout of finFET is

shown in figure 2. The spacermaterials are chosen based on the requirements of performance enhancement. Selecting the proper spacer materials for FinFETs is an important part of the design process since it has an immediate effect on the electrical performance and dependability of the transistor. The dielectric constant, thermal stability, etch selectivity, and suitability for semiconductor manufacturing processes should all be taken into account while selecting spacer materials. The air space is first left free as shown in fig. 1a of 3D schematic view of s-k air space.Various spacer materials are chosen considering the material specificity, its permittivity, thermal characteristics etc., and are analysed. The s-k air space is then filled with different types of spacer elements and analysed. The fig. 1b displays the schematic diagram for the s-k SiO2 spacer. As seen in fig. 1c, 1d, and 1e, nitride, kapton, and HfO2 fill the air gap in the spacer. In FinFET design, the spacer's doping material is crucial for determining transistor characteristics such as leakage current, threshold voltage, and overall design performance. FinFETs require spacer materials to separate the gate electrode from the fin channel in order to prevent undesired leakage currents. The most common spacer materials are silicon oxide (SiO2) and slicon nitride (SiN).The primitive parameter existing in the doping concentration of the spacer material is the threshold voltage which plays an important role to enhance the performance of the device. The threshold voltage represents the minimum voltage required for activating the switching characteristics of the transistor. The presence of the dopants in the spacer material is having the capability to vary the threshold voltage and these variations are used to achieve the good logic levels in Complementary Metal oxide Semiconductor (CMOS) technology. The electrical characteristics of the Source and Drain regions of the transistor based on the parameters threshold voltage and carrier mobility and the concentration of Source-Drain S/D doping is 1E20 atoms/cm^3.The doping concentration represents the flow of holes and electrons of the semiconducting channel which denotes the carrier mobility. The increase in scattering events of the dopant atoms raises doping concentration which reduces carrier mobility. The transistor design mainly depends on the channel length and the density of transistors on a chip. In this paper, the term "fin Pitch" in Fin FET indicates the distance between the fins of the Fin-FET and its value is around 20nm. The Fin-FET design and its architecture is used for evaluating fin pitch and it is calculated by using the center to center distance between adjacent fin structures. This is a simplified example of how fin pitch is calculated:Fin Pitch (P) is equal to the Active Region's Total Width (W) divided by the Fin's Number (N).

$$P = W/N$$

The dimensions of the fin like height and breadth effects the characteristics and functionality of the FinFET. The fin width and height in this design are set at 10nm and these dimensions effects the device performance in terms of speed, power consumption with reference to cutting edge technological nodes.

4. Spacer analysis

a) Single-k Analysis

All of Fig. 1 SiO2 is used as a gate dielectric. The gate electrode and fin channel are detached by the gate dielectric, which acts as an insulating layer. It is essential for allowing the channel's current flow to be controlled, which affects how the transistor behaves. It successfully separates the gate electrode from the channel, stopping unwanted current flow and guaranteeing the transistor operates dependably. Maintaining the transistor's off state and reducing power usage depend heavily on this isolation. Four distinct spacer materials, silicon dioxide (SiO2), silicon nitride (SiN), Kapton, and hafnium dioxide (HfO2) along with air space have been developed in this article. The V-I characteristics shown in fig.3 are derived from a comparison of all spacer materials' drain current analyses with different gate voltages.

Air is found to be the least conductive and have the lowest dielectric constant (k) among naturally occuring spacer materials. It offers the least amount of capacitance possible between related parts. SiO2 is noted for having a low dielectric constant and strong insulating qualities. It is a well-known spacer material with outstanding process compatibility. Since SiN has a greater dielectric constant than SiO2, parasitic capacitance is increased. Polyimide film, or kapton, is a flexible, heat-resistant material that has high chemical stability. It is renowned for having special mechanical qualities. Compared to SiO2, hafnium dioxide has a dielectric

constant that is much higher, making it a high-k dielectric material. It is observed that it has reduced gate leakage and superior electrical qualities. The fig.3 shows the graph of single-k spacer V-I characteristics with linear and log scale. It has been observed that hafnium dioxide achieves high drain current with low gate source voltage.

This makes it easier to come to a conclusion that it can be used as a gate dielectric material rather than SiO2 or other spacer materials which are shown above. Further single-k and dual-k spacers distinguish among each other in terms of V-I characteristics. The selection of spacer materials affects transistor subthreshold swing (SS) variations. Lower SS values are often indicative of higher device performance.

Dual-K Spacer Analysis

Figure 4 shows the 3D schematic view of fully depleted silicon-on-insulator (FDSOI) FinFET of dual-k spacer and the 2D horizontal centre cut in X-Y plane of dual-k spacer. Dual-K spacer in conjunction with (FDSOI) technology provides a powerful and effective foundation for creating cutting-edge semiconductor devices. A thin layer of silicon on a buried oxide layer, which separates the active silicon area from the substrate, is the defining feature of FDSOI. When the transistor is in the off state, its "fully depleted" nature means that all carriers are completely absent from the silicon sheet, greatly reducing leakage current. This is significant with respect to the single-k spacer characteristics. The dimensions of the dual-k spacer of HfO2 are shown in figure 4b and 4c. In Dual-K spacer, the spacer section of a FinFET is designed with two distinct dielectric materials namely HfO2 with high dielectric constant of 20 and SiO2 with dielectric constant of 3.9 in one case as shown in fig.4a and HfO2 and Nitride with dielectric constant value of 8 for SiN in other case as in fig. 4b. To balance process compatibility and performance optimization, SiO2, with its lower k value, is paired with high-k HfO2 in the first instance of a dual-K spacer to fine-tune the electrostatic regulation of FinFET. The decision of HfO2 and SiN is made because the required electrical properties, process compatibility, and particulars of semiconductor design all play a role in the selection of dual-K spacer materials. High-k HfO2 is preferred due to its enhanced electrostatic control and decreased leakage, although SiN, contingent on the application and design objectives, can provide a compromise between process compatibility and performance.

5. Results and discussion

The V-I characteristics of dual-k spacer in two scales are shown in fig.5. It is observed that the nitride with hafnium dioxide has taken off quickly with respect to gate voltage compared to silicon dioxide with hafnium dioxide. This is appropriate for advanced FinFET circuits as it may improve electrical control and lessen short-channel effects. Figure 5(i) shows the linear

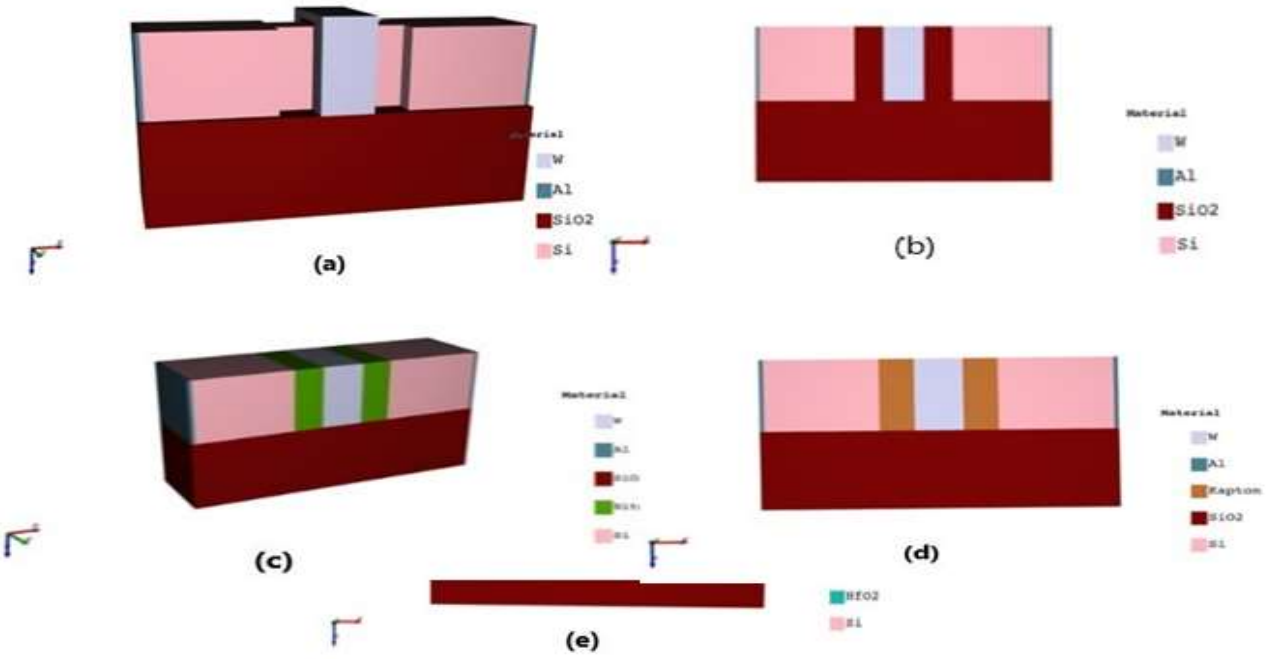


Figure 1: *(a) 3D schematic view of s-k Air space (b) s-k SiO_2 spacer (c) s-k Nitride spacer (d)s-k Kapton spacer (e) s-k HfO_2 spacer.*

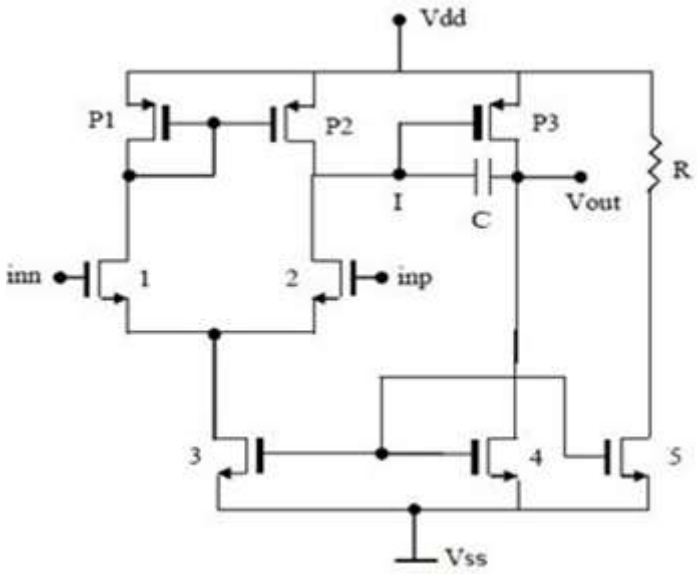
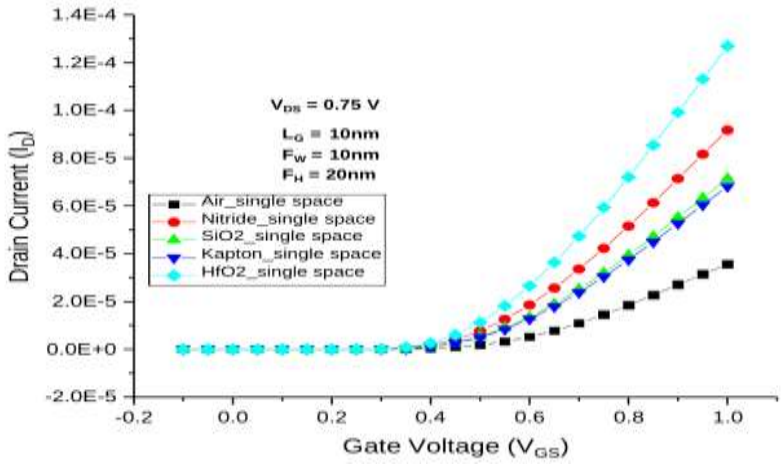
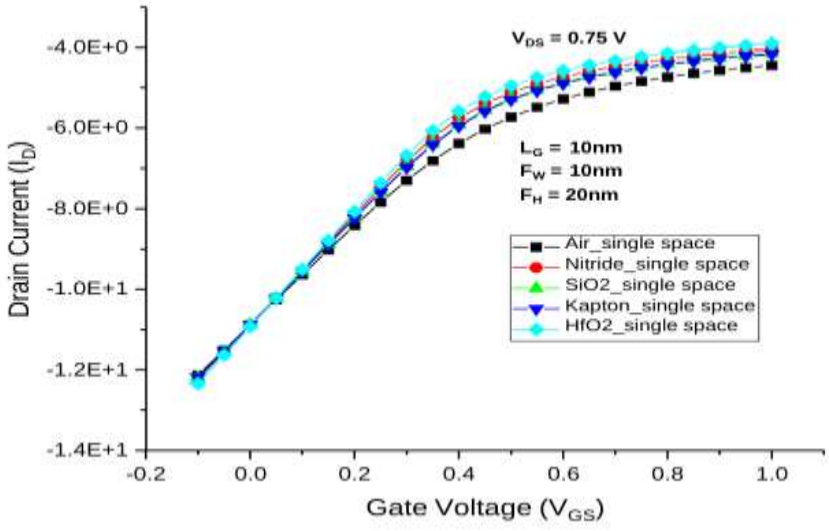


Figure 2: *Interior Layout of FinFET*



(i)



(ii)

Figure 3: *single-k spacer V-I characteristics (i) Linear Scale I_D (ii) Log Scale I_D*

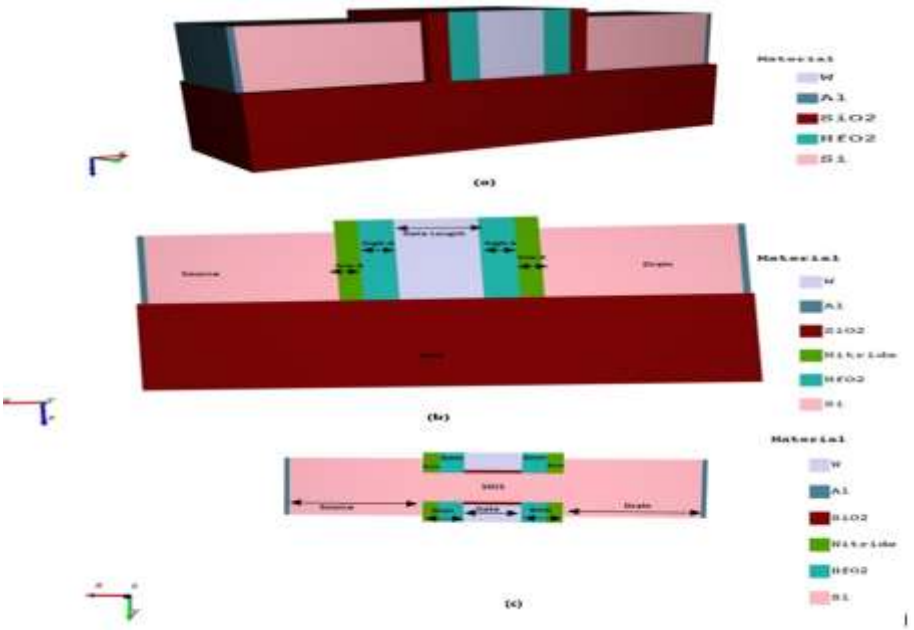
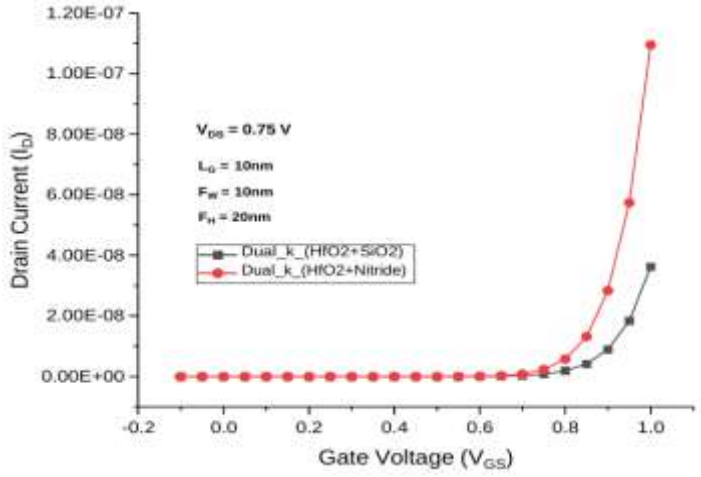
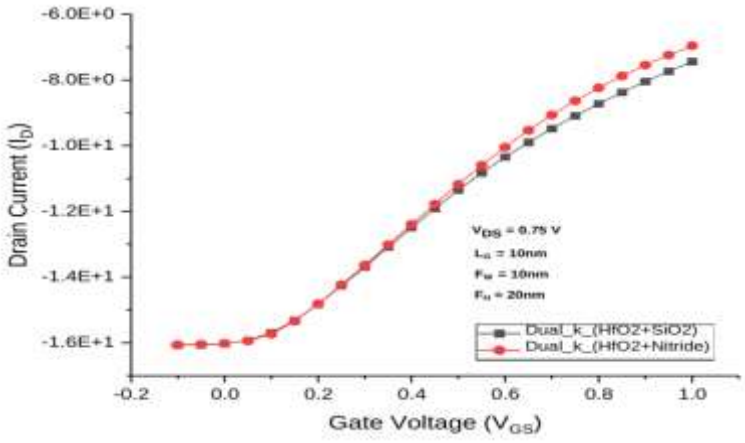


Figure 4: *(a), (b) 3D schematic view of FDSOI FinFET of dual-k spacer (c) 2D horizontalcenter cut X-Y plane of dual-k spacer.*



(i)



(ii)

Figure 5: *V-I characteristics of dual-k spacer in (i) linear scale and (ii) log scale*

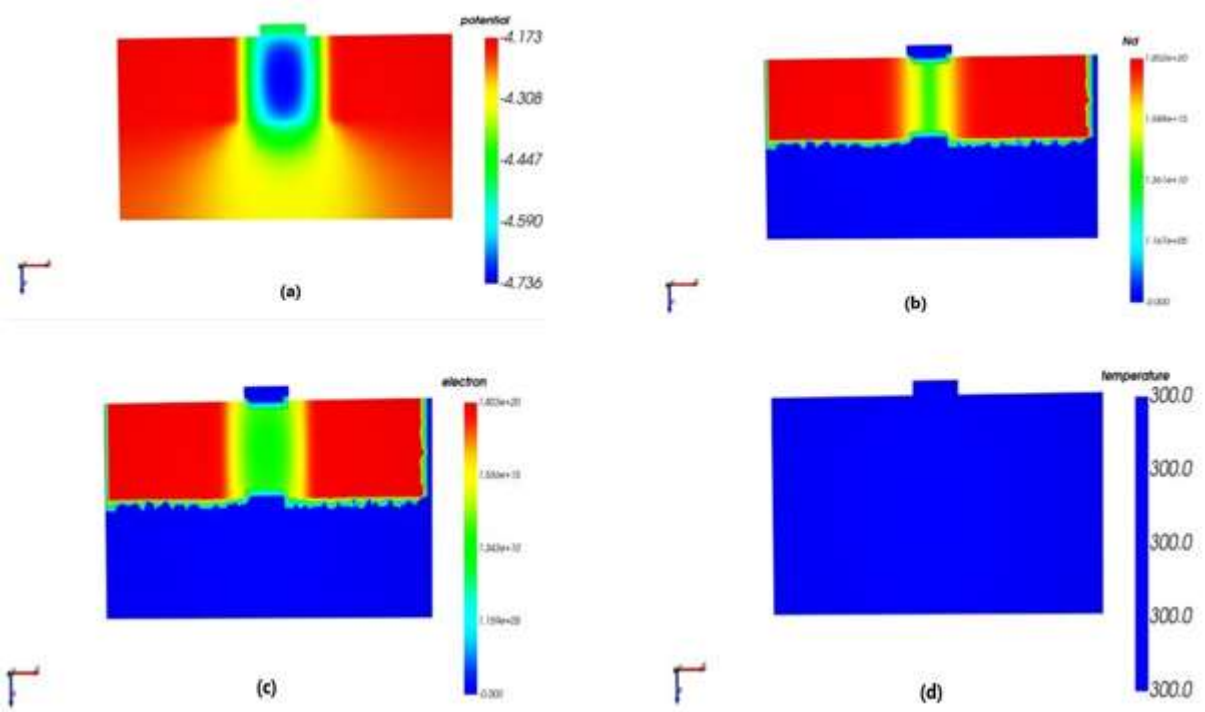


***Figure 6**: (a) The potential of D-k spacer (b) hole concentration of D-k spacer (c) electronconcentration (d) temperature of D-k spacer.*

scale of changes in drain current with respect to changes in gate voltage and figure 5(ii) shows the log scale of the same. It is observed that the HfO2+SiO2 is slow with respect to HfO2+Nitride. The final choice between these dual-K spacer solutions is based on the accepted trade-offs and the particular objectives of the semiconductor device. HfO2 and SiN could be the better option if improving electrical control and mitigating short-channel effects are the main concerns. HfO2 and SiO2 would be a better choice, but, if process compatibility, low parasitic capacitance, and the capacity to sustain device speed are the primary concerns.The potential, hole concentration, electron concentration and the temperature of the fin FET with dual-k spacers is shown in figure 6a, 6b, 6c and 6d respectively. The finFET transistor efficiency is increased by improved control of hole concentration, which also helps to modify threshold voltage and device performance. HfO2+Nitride D-K spacers are useful in controlling electron concentration in n-type transistors in addition to hole concentration in p- type which makes it better to control currents in the drain for both n-type and p-type. Additionally, it is noted that this D-K spacer can assist in reducing temperature-related difficulties, guaranteeing reliable gadget operation in a range of environmental circumstances.

6. Conclusions

One of the key performance characteristics of dual-K spacer FinFETs is the subthreshold swing, which is used to carry out the switching activity of the transistor. This study mainly focuses on single-k- and dual-k-spacer techniques using different dielectric materials. SiO2 spacer, nitride spacer, Kapton spacer, HfO2 spacer are some of the dielectric materials utilised for single- k and dual-k by mixing HfO2 (hafnium dioxide)-nitride materials and HfO2-SiO2 to fine-tune transistor properties. With the help of HfO2+Nitride for Dual-K (D-K) spacer technology, the dual k overcomes the limitations of the single-k spacer method. By managing the concentrations of hole electron carriers, this dual-k technology has the ability to minimize temperature effects.

Dual K spacer technology is used to realize the applications in contemporary advanced semi-conductor fabrication with customization. The substance HfO2+Nitride is taken into consideration by the dual k spacer when implementing device-based applications. This technology mainly optimized design parameters like power, threshold voltage which enhance performance. The device's performance can be improved by decreasing SS values by combining materials with varying K values to control the transistor channel electric field.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
- **Acknowledgement:** The authors declare that they have nobody or no-company to acknowledge.
- **Author contributions:** The authors declare that they have equal right on this paper.
- **Funding information:** The authors declare that there is no funding to be acknowledged.
- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

References

[1] Kaur, N., Gill, S.S. & Kaur, P. (2022) "*Performance Evaluation of Junctionless FinFET"* using Spacer Engineering at 15 nm Gate Length. Silicon 14, 10989–11000. https://doi.org/10.1007/s12633-022-01820-6

[2] V. Chauhan, D. P. Samajdar and N. Bagga,(2022) "*Exploration and Device Optimization of Dielectric–Ferroelectric Sidewall Spacer in Negative Capacitance FinFET*," in *IEEE Transactions on Electron Devices*, vol. 69, no. 8, pp. 4717-4724, doi: 10.1109/TED.2022.3186272.

[3] Y. -K. Lin *et al*.,(2019) "*Spacer Engineering in Negative Capacitance FinFETs*," in *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 1009-1012, doi: 10.1109/LED.2019.2911104.

[4] Mohapatra SK, Pradhan KP, Singh D, Sahu PK (2015) "*The role of geometry parameters and fin aspect ratio of sub-20nm SOI-FinFET: an analysis towards analog and RF circuit design.*" IEEE Trans Nanotechnol 14:546–554. https://doi.org/10.1109/TNANO.2015.2415555.

[5] A. Bhattacharjee, M. Saikiran, A. Dutta, B. Anand and S. Dasgupta,(2015) "*Spacer Engineering-Based High-Performance Reconfigurable FET With Low OFF Current Characteristics*," in IEEE Electron Device Letters, vol. 36, no. 5, pp. 520-522, doi: 10.1109/LED.2015.2415039.

[6] Toledano-Luque, M., Matagne, P., Sibaja-Hernández, A., et al.(2014) '*Superior reliability of junctionless pFinFETs by reduced oxide electric field*', IEEE Electron Device Lett., 35, (12), pp. 1179–1181, https://doi.org/10.1109/LED.2014.2361769.

[7] D. Ryu et al.(2020) "*Design and Optimization of Triple-k Spacer Structure in Two-StackNanosheet FET From OFF-State Leakage Perspective*," in IEEE Transactions on Electron Devices, vol. 67, no. 3, pp. 1317-1322, March 2020, doi: 10.1109/TED. 2969445.

[8] P. K. Dubey and B. K. Kaushik(2017) "*T-Shaped III-V Heterojunction Tunneling FieldEffect Transistor*," IEEE Transactions on Electron Devices, vol. 64, no. 8, pp. 3120-3125, DOI: 10.1109/TED.2017.2715853..

[9] Kumar, R., Devi, B.A., Sireesha, V. et al.(2022) '*Analysis and Design of Novel Doping Free Silicon Nanotube TFET with High-density Meshing Using ML*' for Sub Nanometre Technology Nodes. Silicon. https://doi.org/10.1007/s12633-022-01859-5.

[10] H. Xie and H. Liu,(2020) "*Design and investigation of a dual source and U-shaped gate TFET with n buffer and SiGe pocket*," AIP Advances, vol. 10, no. 5, p. 055125, DOI: 10.1063/5.0006510..

[11] Devi, M.P., Ravanan, V., Kanithan, S. et al.(2022) "*Performance Evaluation of FinFET Device Under Nanometer Regime*" for Ultra-low Power Applications. Silicon 14, 5745–5750. https://doi.org/10.1007/s12633-022-01772-x.

[12] Arun jayakar, S., Rajesh, T., Vignesh, N.A. et al. (2022), "*Performance Analysis of Doping Less Nanotube Tunnel Field Effect Transistor for High Speed Applications. Silicon*" 14, 7297–7304. https://doi.org/10.1007/s12633-022-01839-9.

[13] V. Chauhan, D. P. Samajdar and N. Bagga,(2022) "*Exploration and Device Optimization of Dielectric–Ferroelectric Sidewall Spacer in Negative Capacitance FinFET*," in IEEE Transactions on Electron Devices, vol. 69, no. 8, pp. 4717-4724, Aug. 2022, doi: 10.1109/TED. 3186272.

[14] N. Arun Vignesh, Ravi Kumar, R. Rajarajan, S. Kanithan, E. Sathish Kumar, Asisa Kumar Panigrahy, Selvakumar Periyasamy,(2022) "S*ilicon Wearable Body Area Antenna for Speech-Enhanced IoT and Nanomedical Applications*", Journal of Nanomaterials, vol. 2022, Article ID 2842861, 9 pages. https://doi.org/10.1155/2022/2842861.

[15] Amin, S & Sarin, RK(2016), '*Enhanced analog performance of doping-less dual material and gate stacked architecture of junctionless transistor with high-kspacer*', Applied Physics A, vol. 122, no. 380, pp. 1-9, https://doi.org/10.1007/s00339-016-9904-2.

[16] A. B. Sachid, M. -C. Chen and C. Hu,(2016) "*FinFET With High- κ Spacers for Improved Drive Current*," in IEEE Electron Device Letters, vol. 37, no. 7, pp. 835- 838, doi: 10.1109/LED.2016.2572664.

[17] A. B. Sachid, M. -C. Chen and C. Hu,(2017) "*Bulk FinFET With Low- κ Spacers for Continued Scaling*," in IEEE Transactions on Electron Devices, vol. 64, no. 4, pp. 1861-1864, doi: 10.1109/TED.2017.2664798.

[18] Kanithan, S., Vignesh, N.A., Jana, S. et al. (2022), '*Negative Capacitance Ferroelectric FET Based on Short Channel Effect for Low Power Applications*." Silicon **14**, 9569– 9579. https://doi.org/10.1007/s12633-021-01625-z.

[19] Ludwig et al.,(2003) "*FinFET technology for future microprocessors*," 2003 IEEE International Conference on SOI, Newport Beach, CA, USA, 2003, pp. 33-34, doi: 10.1109/SOI. 1242886.

[20] M. R. Tripathy, A. K. Singh, K. Baral, P. K. Singh, and S. Jit,(2020) "*III-V/Si staggered heterojunction based source-pocket engineered vertical TFETs for low power applications*," Superlattices and Microstructures, vol. 142, p. 106494, DOI:10.1016/j.spmi.2020.106494

[21] A. K. Singh, M. R. Tripathy, S. Chander, K. Baral, P. K. Singh, and S. Jit,(2020) "*Simulation study and comparative analysis of some TFET structures with a novel partial-ground-plane (PGP) based TFET on SELBOX structure*," Silicon, vol. 12, no. 10, pp. 2345-2354, https://doi.org/10.1007/s12633-019-00330-2.

[22] Z. Wei, G. Jacquemod, Y. Leduc, E. d. Foucauld, J. Prouvee, and B. Blampey,(2019)"*Reducing the Short Channel Effect of Transistors and Reducing the Size of Analog Circuits*," Active and Passive Electronic Components, DOI:10.1155/2019/4578501.

[23] T. A. Ameen, H. Ilatikhameneh, P. Fay, A. Seabaugh, R. Rahman, and G. Klimeck,(2019) "*Alloy Engineered Nitride Tunneling Field-Effect Transistor: A Solution for the Challenge of Heterojunction TFETs*," IEEE Transactions on Electron Devices, vol. 66, no. 1, pp. 736-742. DOI: 10.1109/TED.2018.2877753.

[24] Venkatesh M & Balamurugan,(2019), '*New subthreshold performance analysis of germanium based dual halo gate stacked triple material surrounding gate tunnel field-effect transistor*', Superlattices and Microstructures - Elsevier, vol. 130, pp. 485-498, DOI: 10.1016/j.spmi.2019.05.016.

[25] A. Veloso et al., (2023) "Nanosheet-based Device Architectures with Front/Backside Connectivity: Opportunities for S/D Engineering to Enable Advanced CMOS Logic Scaling," 2023 21st International Workshop on Junction Technology (IWJT), Kyoto, Japan, pp. 1-5, doi: 10.23919/IWJT59028. 10175170.

[26] Kumar, E.S., Kumar P, S., Vignesh, N.A. et al. (2022) "*Design and Analysis of Junctionless FinFET with Gaussian Doped for Non-polar Structure.*" Silicon **14**, 8439– 8447. https://doi.org/10.1007/s12633-021-01626-y.

[27] Prakash, M.D., Krsihna, B.V., Satyanarayana, B.V.V. et al. (2022) "*A Study of an Ultrasensitive Label Free Silicon Nanowire FET Biosensor for Cardiac Troponin I Detection*." Silicon **14**, 5683–5690. https://doi.org/10.1007/s12633-021-01352-5.

[28] S. Nandhini, V. R. Palanivelu, Asisa Kumar Panigrahy, N. Arun Vignesh, Ramachandran Kasirajan, (2022) "*ICT System for 14.0 Adoption: Comparative Study to Assess the Readiness in Manufacturing MSMEs*", Journal of Nanomaterials, vol. 2022, Article ID 7595970, 7 pages. https://doi.org/10.1155/2022/7595970.

[29] K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C. Cheng, C.-C. Chen, et al., (2015) "*Sub-60mV-swing negative-capacitance FinFET without hysteresis*", IEDM Tech. Dig., pp. 22.6.1-22.6.4, DOI: 10.1109/IEDM.2015.7409760.

[30] A. B. Sachid, H.-Y. Lin and C. Hu, (2017) "*Nanowire FET with corner spacer for high-performance energy-efficient applications*", IEEE Trans. Electron Devices, vol. 64, no. 12, pp. 5181-5187, https://doi.org/10.1109/TED.2017.2764511.

[31] H. Kim, D. Son, I. Myeong, M. Kang, J. Jeon and H. Shin, (2018) "*Analysis on self- heating effects in three-stacked nanoplate FET*", IEEE Trans. Electron Devices, vol. 65, no. 10, pp. 4520-4526. DOI: 10.1109/TED.2018.2862918.