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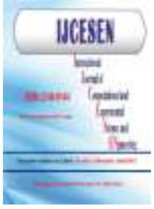

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Research Article

High-Speed Functional Clocks Impact on Vmin (Minimum Operating Voltage) During Scan Testing and Methods to Reduce Vmin

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Abstract:

The Increased focus on Energy Efficiency within the manufacture of Semiconductors is the key leading focus of today's semiconductor manufacturing; voltage level affects equipment power consumption; longevity of that equipment; and ultimately, manufacturer's yield. High-speed functional clocks during scan testing create substantial challenges for voltage optimization. These clocks generate excessive switching activity that elevates voltage requirements beyond normal operational levels. The disparity between testing conditions and functional operation causes unnecessary yield loss. Good chips fail during manufacturing tests despite meeting all functional specifications. Clock gating architectures offer an effective solution to this challenge. Testpoint flops integrated into scan chains enable selective control of functional clock distribution. During capture cycles, strategic disabling of clock gating cells reduces switching activity in critical regions. Silicon validation on advanced process nodes confirms the effectiveness of this technique. Voltage requirements decrease substantially when functional clocks are appropriately managed. The technique scales effectively to future technology nodes where power density challenges intensify. Automated test pattern generation tools can optimize clock gating configurations to balance fault coverage with voltage constraints. The economic benefits are significant for high-volume production. Costs of manufacturing decrease directly due to an increased number of chips that meet voltage testing specifications.

1. Introduction

As the semiconductor industry is currently facing greater-than-ever energy-efficiency issues, the growth rate of AI-based applications continues to be increasing at a pace unlike anything previously seen. Metaverse computing platforms demand immersive experiences with massive computational requirements. These trends have elevated energy consumption concerns to critical levels. Global electricity supply constraints threaten to limit AI deployment at scale. Hardware designers must achieve dramatic improvements in energy efficiency. Some estimates suggest thousand-fold improvements are necessary for truly immersive metaverse experiences.

Digital circuits consume power according to fundamental physical principles. Dynamic power consumption follows the relationship between capacitance, voltage, and frequency. Effective circuit capacitance remains relatively fixed for a given design. Clock frequency determines performance requirements for applications. Supply voltage represents the primary variable for power optimization. Reducing voltage while maintaining performance offers direct energy efficiency gains. This makes voltage optimization a critical design objective.

However, voltage reduction faces physical limitations. Circuit switching delays increase as voltage decreases. Timing margins on critical paths become tighter. Below a certain threshold voltage, timing violations occur. Flip-flops capture incorrect data values. Computational errors result from these timing failures. This threshold defines the minimum operating voltage for correct functionality.

Modern system-on-chip designs prioritize voltage minimization. Pre-silicon design stages employ sophisticated timing analysis tools. Signal integrity verification ensures adequate margins. Power integrity analysis validates voltage delivery networks. These tools help achieve lower voltage targets before fabrication. Post-silicon validation becomes equally important after manufacturing. Real silicon exhibits variations that simulation cannot fully predict.

ATPG-configured embedded enable capture bits have emerged as promising techniques for managing test power. Sun et al. demonstrated that controlling capture operations through embedded configuration bits significantly reduces power consumption during scan testing [1]. Their technique allows selective disabling of scan cell capture operations. This minimizes unnecessary switching activity during test application. The embedded bits get configured by the ATPG tool during pattern generation. This ensures optimal power reduction while maintaining fault coverage requirements.

Structural testing presents specific challenges for voltage management. Sonone and Pradeep identified critical Vmin silicon issues during the manufacturing test [2]. Their analysis revealed that test patterns often create worst-case switching scenarios. These scenarios exceed typical operational conditions significantly. The voltage requirements during the test can be substantially higher than functional operation. This creates yield loss as functionally good chips fail test voltage specifications. They proposed targeted solutions including clock gating and pattern modifications to address these challenges.

This article focuses on the specific voltage challenge during manufacturing tests. High-speed functional clocks during scan testing significantly impact voltage requirements. These clocks create switching activity patterns that differ from normal operation. The resulting voltage elevation causes yield loss in manufacturing. Understanding this phenomenon enables development of effective countermeasures. Section 2 examines voltage challenges in high-performance designs. Section 3 describes functional clock gating architecture for voltage reduction. Section 4 presents experimental results from advanced process nodes. Section 5 discusses implications and future directions. Section 6 provides concluding remarks.

2. Vmin Challenges in Modern High-Performance Designs

2.1 Post-Silicon Voltage Variability

Modern graphics processing units operate at extremely high frequencies. Artificial intelligence applications require gigahertz clock speeds for adequate performance. These high frequencies directly drive dynamic power consumption. Each clock cycle triggers switching events throughout the circuit. Capacitive loads charge and discharge repeatedly. The cumulative effect creates substantial power demand.

Manufacturing tests introduce unique challenges for voltage management. Scan testing applies transition patterns to detect fabrication defects. These patterns exercise circuit paths systematically to achieve high fault coverage. Functional clocks exceeding one gigahertz continue operating during test capture cycles. The combination of scan activity and functional clock toggling creates extreme switching scenarios.

Post-silicon profiling reveals significant voltage variability across complex digital logic. Chen analyzed Vmin variability through comprehensive silicon characterization [3]. The profiling identified multiple sources of voltage variation. Process variations create device-to-device differences. Local manufacturing variations affect threshold voltages. Temperature gradients across the die impact performance. Voltage droop from switching activity varies by location. These factors combine to create complex voltage landscapes across chips.

The profiling methodology employs adaptive voltage scaling during the test. Critical paths get identified through systematic voltage reduction. Failing paths reveal voltage-sensitive regions. Statistical analysis quantifies variability distributions. This data guides design improvements for subsequent revisions. The profiling also validates pre-silicon predictions. Correlation between simulation and silicon identifies modeling gaps.

Low power aware ATPG techniques address test power concerns systematically. Raviraj D explored power-aware pattern generation for scan-based testing [4]. Traditional ATPG focuses exclusively on fault coverage maximization. This often generates patterns with excessive switching activity. Power-aware ATPG incorporates switching activity as an optimization objective. The tool balances coverage requirements with power constraints. Techniques include don't-care bit filling to minimize transitions. X-bit assignment strategies reduce capture power. Clock gating integration provides additional control mechanisms.

2.2 Manufacturing Yield Impact

The voltage discrepancy between test and operation creates economic consequences. Chips functioning correctly at normal voltages fail during the manufacturing test. These failures occur despite chips meeting all functional specifications. The test environment creates artificial worst-case scenarios. Good silicon gets discarded due to test-induced voltage violations.

Process node scaling exacerbates this challenge. Two-nanometer processes and beyond exhibit dramatically increased power density. Current delivery becomes more difficult. Resistance in power distribution networks increases. Voltage margins become tighter. Small switching activity increases cause disproportionate voltage impacts.

The economic implications extend beyond immediate yield loss. Test costs increase when additional voltage margin must be provided. Higher test voltages may require specialized equipment. Binning strategies become more conservative to ensure reliability. Product qualification becomes more challenging with larger voltage gaps.

2.3 Test Environment Characteristics

The test environment differs fundamentally from normal operation. Functional workloads exhibit predictable patterns. Power management systems optimize voltage and frequency dynamically. Applications rarely exercise worst-case switching simultaneously across all circuit blocks. Real-world usage patterns allow voltage optimization.

Manufacturing test cannot make these assumptions. Fault coverage requirements dictate pattern characteristics. Patterns must detect manufacturing defects wherever they occur. This necessitates exercising many circuit paths simultaneously. Switching activity becomes uniformly high across the chip. All clock domains may toggle simultaneously during capture. This creates power consumption scenarios that never occur during normal use.

Several factors compound the voltage challenge. Scan chains themselves add switching overhead. Long scan chains toggle many flip-flops during shift operations. Functional clocks continue operating during capture windows. Automatic test pattern generation tools prioritize fault coverage over power optimization. The cumulative effect pushes voltage requirements beyond acceptable limits. Temperature effects during test differ from operational conditions. At-speed testing requires high frequency operation without thermal equilibrium.

3. Functional Clock Gating Architecture for Vmin Reduction

3.1 Scan Cell Output Blocking Techniques

Effective voltage management during scan testing requires architectural innovation. Clock gating provides a proven mechanism for power control during functional operation. Extending clock gating principles to test scenarios offers a solution. The key innovation involves controlling clock gating cells during scan capture operations.

Blocking scan cell outputs represents a fundamental approach to power reduction. Lin and Rajski developed techniques for selectively disabling scan cell outputs during test [5]. Their method prevents unnecessary transitions from propagating through combinational logic. Scan cells get configured to block output changes during specific cycles. This reduces switching activity in downstream logic cones. The blocking mechanism employs additional control logic at scan cell outputs.

The technique operates transparently to fault coverage. Critical paths for fault detection remain active. Non-critical paths get blocked to reduce power. The ATPG tool identifies which cells can be blocked safely. Pattern generation accounts for blocking constraints. Fault coverage remains identical to traditional testing. Only switching activity decreases through selective blocking.

Implementation requires modest design modifications. Each scan cell receives an additional blocking control signal. The control signal gets loaded during scan shift operations. Multiplexing logic selects between normal and blocked operation. The area overhead remains minimal compared to total scan infrastructure. Routing resources for control signals require careful planning.

Static compaction techniques provide complementary power reduction. Sankaralingam et al. developed compaction methods that control scan vector power [6]. Traditional test compaction focuses on reducing pattern count. Power-aware compaction considers switching activity during merging decisions. Patterns with similar switching characteristics get grouped together. This enables consistent power management across compressed pattern sets.

The compaction process analyzes each pattern's power signature. Switching activity gets calculated for all scan cells. Patterns get clustered based on power profiles. Merging decisions favor low-power combinations. Don't-care bits get filled to minimize switching. The resulting compressed patterns maintain low power characteristics. Test time reduction combines with power optimization benefits.

3.2 Design Architecture Implementation

The architecture integrates testpoint flops into scan chains. These testpoint flops serve as control points for clock gating cells. Each testpoint flop connects to one or more clock gating cell enable inputs. During scan shift operations, the test pattern loads specific values into testpoint flops. These values determine which clock gating cells remain active during capture.

At the completion of scan shift, testpoint flops hold their loaded values. The subsequent capture cycle uses these values to gate functional clocks. Disabled clock gating cells prevent clock propagation to downstream flip-flops. This selectively reduces switching activity in chosen circuit regions. Power consumption decreases proportionally to the number of disabled clocks.

Successful implementation requires careful design planning. The distribution of clock gating cells must be analyzed thoroughly. Each clock gating cell controls a specific number of sequential elements. Load balancing across clock gating cells affects control granularity. Too few clock gating cells limits regional control. Too many increases area overhead and complexity.

The number of sequential elements per clock gating cell determines switching activity reduction effectiveness. Balanced distribution provides optimal results. Regions with higher switching activity benefit from finer-grained control. Less active regions can tolerate coarser clock gating granularity. This balance must be established during design phases.

3.3 Silicon-Guided Optimization Strategy

Initial silicon testing provides critical feedback for optimization. First silicon devices undergo comprehensive scan testing. Voltage shmoo analysis identifies problematic patterns and conditions. Regions exhibiting voltage sensitivity become visible through failure analysis. This data reveals hotspots where switching activity most impacts voltage.

Armed with hotspot identification, clock gating can be targeted effectively. Testpoint values get configured to disable clocks in problematic regions. Subsequent testing validates the effectiveness of selective clock gating. Iterative refinement continues until voltage requirements meet targets. This silicon-guided optimization maximizes voltage reduction while preserving fault coverage.

The approach maintains flexibility across different pattern types. Each test pattern can configure clock gating independently. Patterns targeting specific fault models may require different switching profiles. Stuck-at fault patterns might tolerate more switching activity. Transition delay patterns might need aggressive clock gating. The testpoint architecture accommodates these varying requirements.

Clock domain analysis guides optimization decisions. Different clock domains exhibit varying voltage sensitivity. High-frequency domains typically show greater voltage impact. Lower frequency domains may operate without aggressive gating. The optimization targets the most sensitive domains first. This provides maximum benefit with minimal coverage impact.

4. Experimental Results from Advanced Process Nodes

4.1 X-Filling Heuristics for Peak Power Reduction

Experimental validation occurred on advanced process node test chips. The test vehicles implemented various power reduction architectures. Testpoint flops controlled clock gating cells throughout the designs. Multiple scan patterns exercised various circuit paths and fault types.

Peak power consumption during scan testing presents critical challenges. Badereddine et al. investigated test pattern modification with X-filling heuristics [7]. Their techniques target peak power minimization during capture cycles. Don't-care bits in test patterns provide optimization opportunities. Strategic filling of X-bits reduces simultaneous switching activity. The heuristics analyze circuit structure to guide filling decisions.

Multiple X-filling strategies exist with different optimization goals. Minimum transition fill minimizes total switching activity. Adjacent fill reduces switching between consecutive patterns. Weighted transition fill considers circuit topology. The effectiveness varies by design characteristics and pattern types. Hybrid approaches combine multiple strategies for robust results.

Silicon measurements validated the peak power reduction effectiveness. Test patterns with optimized X-filling showed substantially lower peak current. Voltage droop during capture decreased measurably. Temperature rise during test reduced significantly. These improvements translated directly to lower voltage requirements. Chips passed testing at voltages closer to functional operation.

4.2 Silicon Validation Results

Silicon testing occurred on automated test equipment. Voltage shmoo experiments varied supply voltage across a range. Each voltage point underwent pattern application and result checking. Pass/fail boundaries defined the minimum voltage for correct operation. These experiments repeated for patterns with and without power management.

Transition patterns received particular attention. These patterns create high switching activity by design. Consecutive capture cycles apply opposite values to flip-flops. This maximizes switching on circuit paths between flip-flops. Transition patterns typically exhibit the highest voltage requirements during scan testing.

Initial experiments established baseline voltage requirements. Patterns executed without selective clock gating control. All functional clocks remained active during capture cycles. This represents traditional scan testing methodology without power optimization. Results showed elevated minimum voltage requirements compared to functional operation.

Subsequent experiments activated the power management mechanisms. Testpoint flops loaded values to disable selected clock gating cells. X-filling heuristics optimized don't-care bit assignments. Voltage noise aware pattern generation sequenced test application. The percentage of active clocks varied across different experimental conditions.

Results demonstrated substantial voltage reduction across all techniques. Patterns with comprehensive power management showed dramatically lower minimum voltage. The passing voltage window widened considerably. Chips previously failing at nominal test voltages now passed successfully. The yield improvement translated directly from voltage reduction. Statistical analysis quantified the voltage margin improvement.

4.3 Pattern-Specific Optimization Results

Different pattern types responded differently to power management techniques. Transition patterns showed maximum benefit from clock gating control. These patterns naturally create high switching activity. Reducing functional clock activity provided substantial voltage relief. The voltage reduction reached significant levels with aggressive clock gating.

Stuck-at patterns showed more modest improvements. These patterns exercise fewer transitions during capture. Switching activity starts lower than transition patterns. Clock gating still provided benefits but smaller in magnitude. The voltage reduction remained worthwhile for yield improvement. X-filling heuristics contributed more to stuck-at pattern optimization.

Path delay patterns exhibited intermediate behavior. These patterns create transitions on long paths while minimizing others. Targeted clock gating on specific paths provided good results. Other paths maintained clocking for proper fault excitation and propagation. The voltage noise aware generation proved particularly effective for path delay testing.

The optimal strategy combines multiple techniques. Clock gating addresses functional clock switching. X-filling optimizes scan cell transitions. Voltage noise aware generation manages overall power profiles. Pattern ordering sequences tests for thermal management. This comprehensive approach maximizes voltage reduction while maintaining complete fault coverage.

5. Discussion and Future Directions

5.1 Hybrid Test Pattern Strategies

The voltage reduction achieved through power management delivers substantial economic benefits. Manufacturing yield improvement directly impacts profitability. Advanced process nodes involve extremely high wafer costs. Each additional passing chip significantly affects manufacturing economics. Consider high-volume production scenarios. Even small percentage improvements in yield produce large absolute gains.

Hybrid test patterns combining external and built-in self-test offer additional opportunities. Das et al. demonstrated test data volume reduction using hybrid approaches [9]. Their technique leverages both deterministic external patterns and pseudo-random BIST patterns. External patterns target difficult faults requiring specific values. BIST patterns provide high coverage for random-testable faults. The combination reduces pattern count while maintaining coverage.

The hybrid approach benefits voltage management in multiple ways. BIST patterns inherently exhibit more uniform switching activity. Random patterns avoid worst-case switching scenarios common in deterministic patterns. External patterns get optimized specifically for power and coverage. The BIST portions run at controlled power levels. Pattern count reduction decreases cumulative test power and thermal effects.

Implementation requires coordination between external and internal test modes. The test controller switches between modes during test application. Fault simulation validates coverage across both pattern sources. The BIST hardware requires modest area investment. Configuration registers control BIST operation parameters. Results get compared through signature analysis or direct comparison.

Test resource partitioning enables efficient system-on-chip testing. Chandra and Chakrabarty developed optimization methods for test resource allocation [10]. Large SoCs contain numerous cores requiring concurrent testing. Resources include scan channels, pattern memory, and test time. Optimal partitioning balances multiple objectives simultaneously. Power constraints limit concurrent test operations. Voltage delivery capability restricts active core combinations.

5.2 Future Technology Directions

The partitioning algorithm considers power as a primary constraint. Each core's test power characteristics get profiled. Concurrent testing combinations must satisfy total power limits. Scheduling sequences tests to manage thermal effects. The optimization minimizes test time while respecting power budgets. Clock gating integration provides additional flexibility for power management.

The clock gating approach scales effectively to future technology nodes. Sub-two-nanometer processes face even greater power delivery challenges. Current density limits become more restrictive. Resistance in interconnect increases. Voltage margins continue shrinking. These trends make voltage management during test increasingly critical.

Advanced packaging technologies introduce additional considerations. Three-dimensional integration stacks multiple dies vertically. Power delivery through silicon vias creates new challenges. Thermal management becomes more complex. The clock gating approach adapts to these scenarios. Each die can implement independent clock gating control. Through-silicon-via power delivery benefits from reduced switching activity.

Chiplet-based designs also benefit from the architecture. Modern systems-in-package integrate multiple chiplets. Each chiplet may come from different sources. Standardizing on clock gating for voltage control enables interoperability. Test methodologies remain consistent across chiplets. This facilitates system-level test development. Inter-chiplet interfaces require special attention for power management.

5.3 Machine Learning Integration

Future enhancements could incorporate machine learning techniques. Because large amounts of testing data exist and have many hidden relationships and patterns within them, Machine Learning algorithms are the most effective means of determining those relationships and finding those patterns. Intelligent systems provide multiple opportunities for optimizing operations within the manufacturing process.

Predictive models could forecast voltage requirements from design characteristics. Training on historical silicon data builds understanding of voltage drivers. New designs get analyzed to predict likely hotspots. This enables proactive design modifications before fabrication. The models learn relationships between design features and voltage sensitivity. Early prediction guides design-for-test insertion decisions.

Adaptive testing algorithms could adjust power management in real-time. On-chip voltage sensors provide feedback during test execution. Machine learning models process sensor data continuously. Dynamic adjustments to clock gating respond to observed conditions. This accommodates die-to-die variation automatically. Fast corner devices use less aggressive power management. Slow corner devices employ maximum power reduction.

Pattern generation optimization could employ reinforcement learning. The optimization space for power management is large and complex. Traditional optimization algorithms may miss optimal solutions. Reinforcement learning explores the space more thoroughly. The learned policies generalize across similar design blocks. Training occurs on representative designs. Deployment applies learned strategies to new designs.

Table 1: *Vmin Challenges and Variability Sources in High-Performance Designs [3, 4]*

Challenge Category	Impact on Voltage Requirements	Mitigation Approach
Process Variations	Device-to-device threshold voltage differences create voltage uncertainty	Post-silicon profiling to identify critical paths
Manufacturing Variations	Local fabrication inconsistencies affect performance characteristics	Adaptive voltage scaling during test execution
Temperature Gradients	Thermal distribution across die influences switching delays	Power-aware ATPG with thermal considerations
Voltage Droop	Location-dependent switching activity causes regional voltage drops	Statistical analysis and design improvements

Table 2: *Clock Gating Architecture Components and Control Mechanisms [5, 6]*

Architecture Element	Functional Role	Design Consideration
Testpoint Flops	Control clock gating cell enable signals during capture	Placement within scan chains affects routing complexity
Scan Cell Output	Prevents unnecessary transitions	Additional control logic at scan cell

Blocking	in combinational logic	outputs required
Clock Gating Cells	Selectively disable functional clock propagation	Load balancing across cells determines control granularity
Static Compaction	Groups patterns with similar switching characteristics	Merging decisions favor low-power combinations

***Table 3**: Power Reduction Techniques and Silicon Validation Outcomes [7, 8]*

Technique Applied	Implementation Method	Observed Benefit
X-Filling Heuristics	Strategic don't-care bit assignment to minimize transitions	Lower peak current and reduced voltage droop
Voltage Noise Aware ATPG	Supply network modeling during pattern generation	Distributed switching activity prevents local voltage droop
Selective Clock Gating	Testpoint-controlled disabling of clock domains	Widened passing voltage window for manufacturing test
Pattern Ordering	Sequential arrangement considering thermal effects	Reduced temperature rise and voltage requirements

***Table 4**: Hybrid Test Strategies and Future Technology Integration [9, 10]*

Strategy Component	Technical Implementation	System Benefit
External Pattern Optimization	Deterministic patterns targeting difficult faults	Power-optimized coverage for complex defects
Built-In Self-Test Integration	Pseudo-random patterns for random-testable faults	Uniform switching activity avoids worst-case scenarios
Test Resource Partitioning	Power-constrained concurrent core testing	Minimized test time while respecting power budgets
Machine Learning Enhancement	Predictive modeling from historical silicon data	Proactive design modifications and adaptive control

6. Conclusions

Energy efficiency dominates modern semiconductor design priorities. Minimum operating voltage directly determines power consumption and device longevity. High-speed functional clocks during manufacturing test create substantial voltage challenges. Excessive switching activity elevates voltage requirements beyond normal operational levels. This voltage gap causes unnecessary yield loss as good chips fail artificial test conditions. Clock gating architectures provide an effective solution to this manufacturing challenge. Testpoint flops integrated into scan chains enable selective control of functional clock distribution during capture cycles. Strategic disabling of clock gating cells reduces switching activity in voltage-sensitive regions without compromising fault coverage. X-filling heuristics optimize don't-care bit assignments to minimize peak power consumption. Silicon validation on advanced process nodes demonstrates substantial voltage reduction effectiveness. The technique scales naturally to future technology nodes where power density challenges continue intensifying. Manufacturing costs decrease significantly as more chips pass voltage specifications during testing. Hybrid test approaches combining deterministic patterns with built-in self-test offer additional optimization opportunities. Test resource partitioning enables efficient concurrent testing while respecting power constraints. Machine learning integration promises enhanced optimization through predictive modeling and adaptive control. The economic benefits prove substantial for high-volume production where each percentage point of yield improvement affects profitability significantly. As semiconductor manufacturing progresses toward increasingly advanced process nodes, comprehensive voltage management during test becomes essential for competitive success.

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