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Research Article

An Efficient Nano Scale Sequential Circuits with Clock Inherent Capability In QCA For Fast Computation Paradigm

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E tool.

Abstract:

Quantum-Dot Cellular Automata is a cutting-edge nanotechnology emerging in the globe, has supplanted the conventional CMOS technologies. Because it doesn't use electric current, this method uses less power because of the Coulomb interaction. This sequential circuit design concept is the most challenging approach in the field of QCA technology. In this proposed study, to design a novel D type flip-flop with pulse generator is included. This plan involves the design of n-bit counter using frequency divider approach. In this approach a novel D flip-flop worked with pulse generator. The QCA Designer, which compares the simulation findings with the suggested constructed circuits, is used to implement the suggested technique. The QCA Designer E tool is used to verify the power usage, which forms the basis of the performance analysis. The suggested plan provides the lowest power and improved performance factors based on the examination of the current approaches.

1. Introduction

As the integration density increased, CMOS technology introduced a novel adjustment to the scaling factor [1-7]. The complexity level climbs as a transistor size decreases, leading to an increase in power depletion and consistency variables examined by Compano R et al [8]. QCA Technology and CNTs (Carbon Nanotubes) are examples of innovative nanotechnology designs that use a number of elements to get over current flaws. Because electric current, which tends to transport information about the logic processes, is eliminated when using QCA technology, power consumption is minimal. Less than the channel length of the CMOS production process, the proposed QCA Technology has characteristics like the 2–18 nm length examined.

According to Amlani et al. [3], the Quantum-Dot Cellular Automata Technology's range is typically measured in THz. The primary component utilized in the construction of sequential circuits is flip-flop (FF). QCA technology reduces the reliability challenges associated with circuit design and synchronous factors in sequential circuits. Numerous studies were conducted in the realm of design with regard to the Flip Flop (FF) design. The area and latency variables are the primary determinants of Flip Flop design, which suggests a reduction in power usage. Flip Flop (FF) is designed using Quantum-Dot Cellular Automata (QCA) Technology without taking into account any regular or symmetrical designing structures. Technical issues like the same circuit having a different Flip Flop (FF) occur from the inconsistencies in the varied Flip Flop (FF) designs. The main difficulty that leads to increased area consumption and latency issues is the interconnection of different Flip Flops (FF) kinds.

Numerous surveys have been conducted based on the data and computational examination of the system, which is known as processing-by-wire and memory-in-motion by Amlani et al. [3]. Registers and counters make up the majority of sequential circuits, which are often utilized in the design industry [9-31]. The two components of the system—counting pulses and dividing frequency—are what make counters unique. Yang et al. [32] conducted a number of surveys about the examination of traditional designs utilized in digital systems. With the use of D type Flip Flop and a pulse generator circuit, the suggested article suggests a revolutionary robust QCA design. Lastly, counters based on frequency dividers using the single layer approach are built.

The following portion of this article will provide a detailed explanation of D type Flipflop with pulse generator in QCA Design. The proposed research with existing designs is presented in Sections II. With the help of proposed D type Flip-flop to design a synchronous counter is presented in section III. The section IV covered the results for the proposed designs. In Section V, conclusions and discussions on potential future implementation strategies were conducted.

2. Research Approach

2.1 Existing QCA Designs for Different Types of Flip-Flops

Sequential circuit execution in QCA technology is dependent on a number of factors, including consistency, low power consumption, and fast speed, as examined by Sheikhfaal et al. [21]. Because of its synchronous mechanism and complicated architecture, QCA technology offers a wide range of current applications compared to sequential technology. The power consumption will be low since sequential circuits are becoming more and more important. Flip-Flop contributes significantly to the system's relevance in this sequential circuit. In existing design in Flip-Flop, few designs used line-based or loop-based structural design due to changes in the inherent capabilities. The design should be classified as either loop-based or line-based as the goal is to reduce the complexity.

2.2 Earlier D Type Flip-Flop

The D type flip flop, which is made of wire with delay, is a component of QCA technology. However, building a sequential circuit is inefficient. due to limitations in timing and synchronization when putting sequential circuits into practice. A clock is connected to QCA flip flops via an external input in order to alter the cause. The D flip flop is coupled with QCA technology based on such limitations. The concept's implementation is displayed below. The D-FF level triggered version of QCA in Vetteth et al. [29] has a loop-oriented structure and The QCA D-FF technology is optimized using a coplanar wire crossing method. Figure 1 illustrates the QCA layout graphically. Crossover wires are absent from the meanwhile loop-oriented D-FF constructed with 90° QCA cells, as seen in Figure 2,3 and 4, respectively. The design of the QCA multiplexer is loop-oriented. Figure 5 and 6 shows the flip-flop design using majority gate that was presented in Rezaei et al. [19] and Abutaleb [1]. Compared to flip flops with line-based designs, it contains fewer cells.

Figure 1. *Presented in [9].*

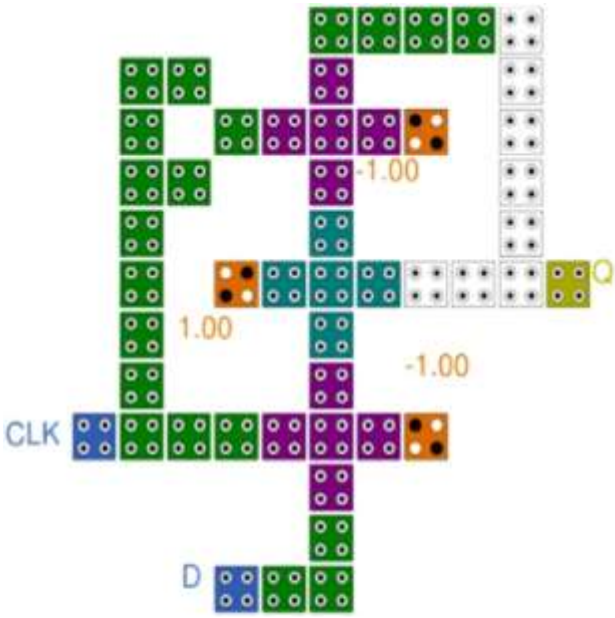


Figure 2. *Presented in [11].*

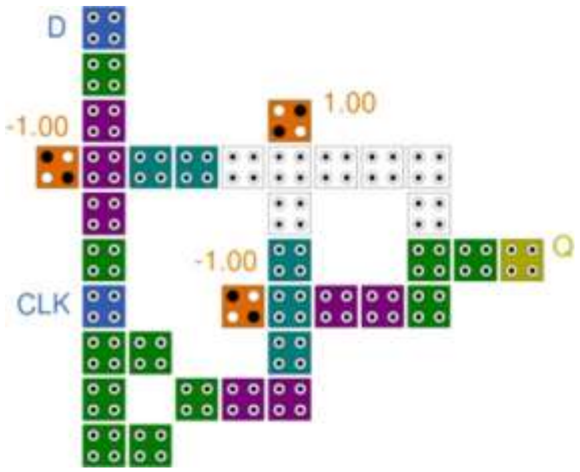


Figure 3. *Presented in [13].*

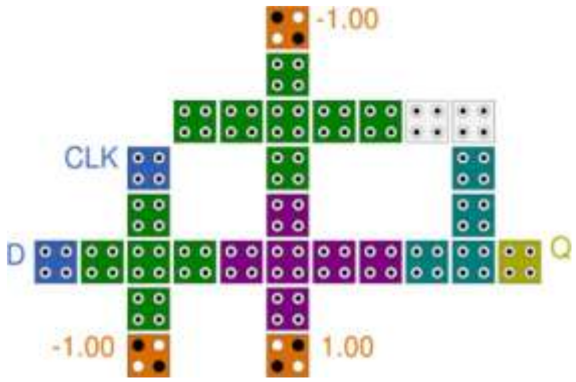


Figure 4. *Presented in [21].*

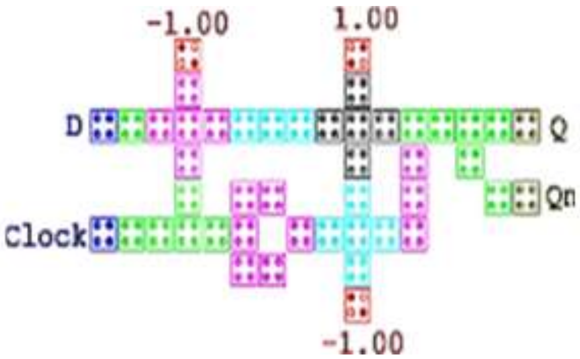


Figure 5. *Presented in [23].*

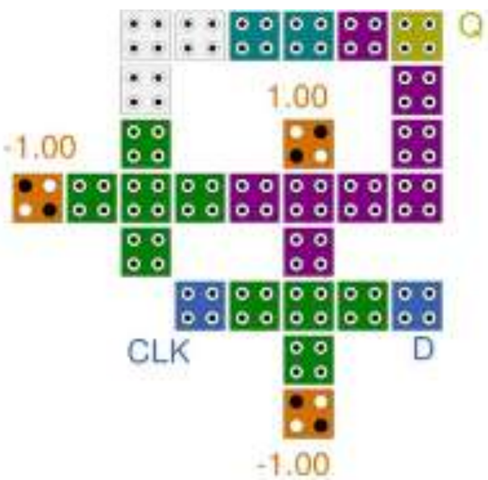


Figure 6. *Presented in [31].*

2.3 Suggested design D-type flip-flop

In the implementation of QCA, a pulse generator with D-FF is introduced. With a clock input, the counter measures rely on a frequency divider. Figure 7(a), 7(b), and 7(c) illustrate the a graphic symbol and a gate and majority gate based structure, whereas D and CLK were the inputs containing memory elements. It has several functions, such as converting D into Q and maintaining Q. Eq. (1) expresses the creation of logical functions pulses in D-FF. Eq. (2) illustrates how the formulation of the design equation depends on the majority voter gates, which are essential components of QCA circuits.

$$Q = (D.\ clk) + (Qt\text{-}1\ .clk) \qquad (1)$$

$$Q = Majority\ (Majority\ (\ D,clk,0)\ Majority\ (\ Qt\text{-}1,clk,0),\ '1') \qquad (2)$$

Table 1 displays the D-FF implementation. According to the table, input D stores in output Q cause 1 to stimulate the CLK (clock). And when CLK is inverted by 0, the output stays the same. The pulse generator's QCA architecture with D-FF in Figure 8 calls for several gates connected by two subsequent gate-levels.

Table 1. *Truth Table for D FF.*

Clk	Data Input	Qt	State
0	0	Qt-1	Hold
0	1	Qt-1	Hold
1	0	0	Transparent
1	1	1	Transparent

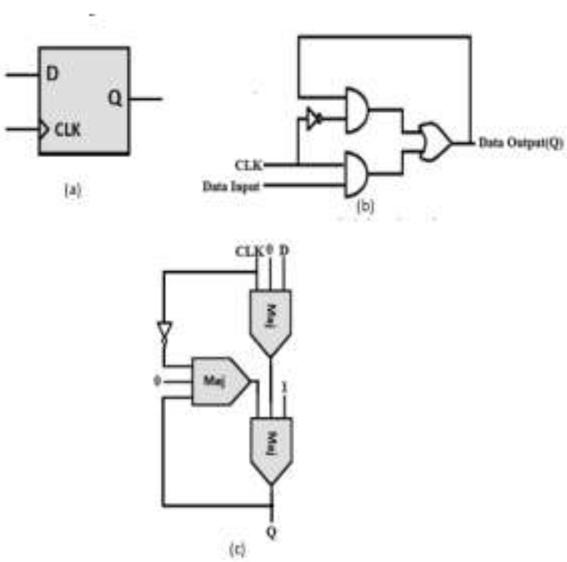


Figure 7. *Proposed Designs of D type Flip-flop (a) Pictogram (b) Circuit Diagram using logic gates (c) Circuit diagram using Majority Gates.*

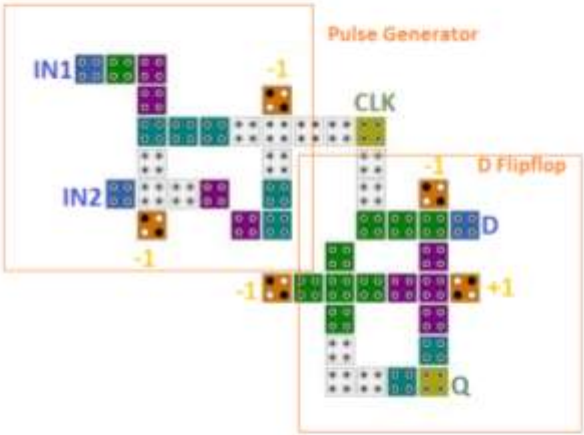
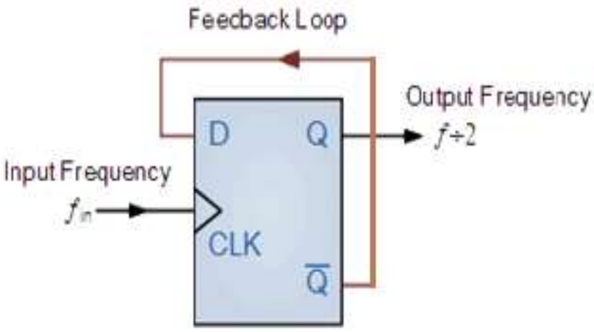


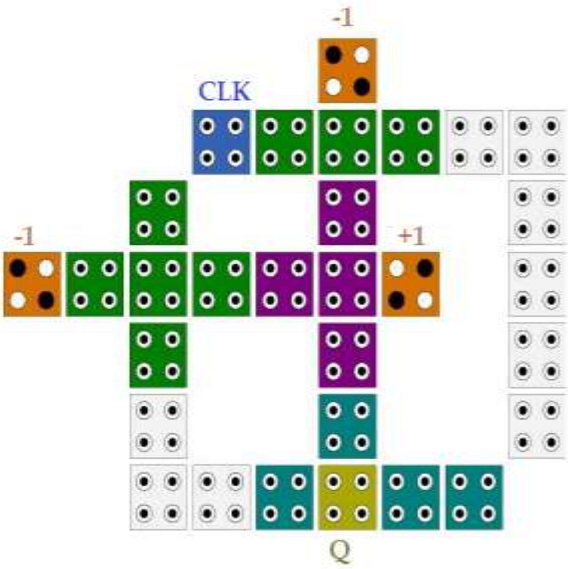
Figure 8. *Suggested QCA layout for D FF with pulse generator.*

3. Suggested Designs in Counter

3.1 Concept of Divide-by-2 Counters



(a) Circuit Diagram



(b) Proposed Design
Figure 9. *Divide-by-2 counters.*

While logical and digital circuits provide a way to reduce the input pulse train by two factors, it can also do D type logic flip flops. In this concept the Qbar output for D flip-flop is connected to the input. This straightforward method of training pulses from the arriving side functions as a clock for the device, data for the D input, and a clock for the output. If Q output level 1 is present, it indicates that Qbar output is 0. Additionally, the output turns to 0 as the data is clocked through output Q on the subsequent positive edge. The Qbar output is timed one more after repeating. Additionally, it is the reverse of Q output in that the states change periodically as output varies. On the positive going edges of the approach heartbeat clock stream, it is typically observed that the circuit's yield just changes states. Per positive edge occurs once per cycle, with the exception that the D-type circuit's yield requires two changes to complete a cycle. This suggests that the yield from the D-type circuit varies at a significant rate that corresponds to the upcoming cardiac pulse train. That is, it has been split in half. Figure 9(a) and 9(b) show the QCA-based divide by two counter schematic and QCA design.

3.2 n-bit Asynchronous Counter

The n-bit asynchronous counter is the primary component of the suggested approach. The clock synchronization pulses that are utilized to construct the 2n counter and n-bit asynchronous counter that makes up the counter. Through the circuits' level, which is shown as D-FF, the noise level during the clock signal is reduced. The register or pattern generator, which is a feature of a specific output based on different binary sequences, is primarily responsible for the counter analysis's fast speed, low power consumption, and consistency. The clock signal is a representation of the binary sequence that serves as an input signal. Data is sent from the input system to the output system using this clock signal.

The categorization range of the synchronous counter and the asynchronous n-counter is determined by the increase in the count value as one or many. Counters, often known as "cascaded" or "divide by n counters," are created by connecting n input signals to the output signal; the number n in the counter denotes the number of stages in the counter base. The modulus, or "MOD," which counts the output states that return the input value itself, is represented by the two phases above. The following n-bit asynchronous counter employing the frequency divider principle, as illustrated in Figure 10, makes up the diagrammatic representation of the suggested work. Figures 11(a) and 11(b) in this study show the suggested design for a 2 bit and n-bit counter in QCA technology

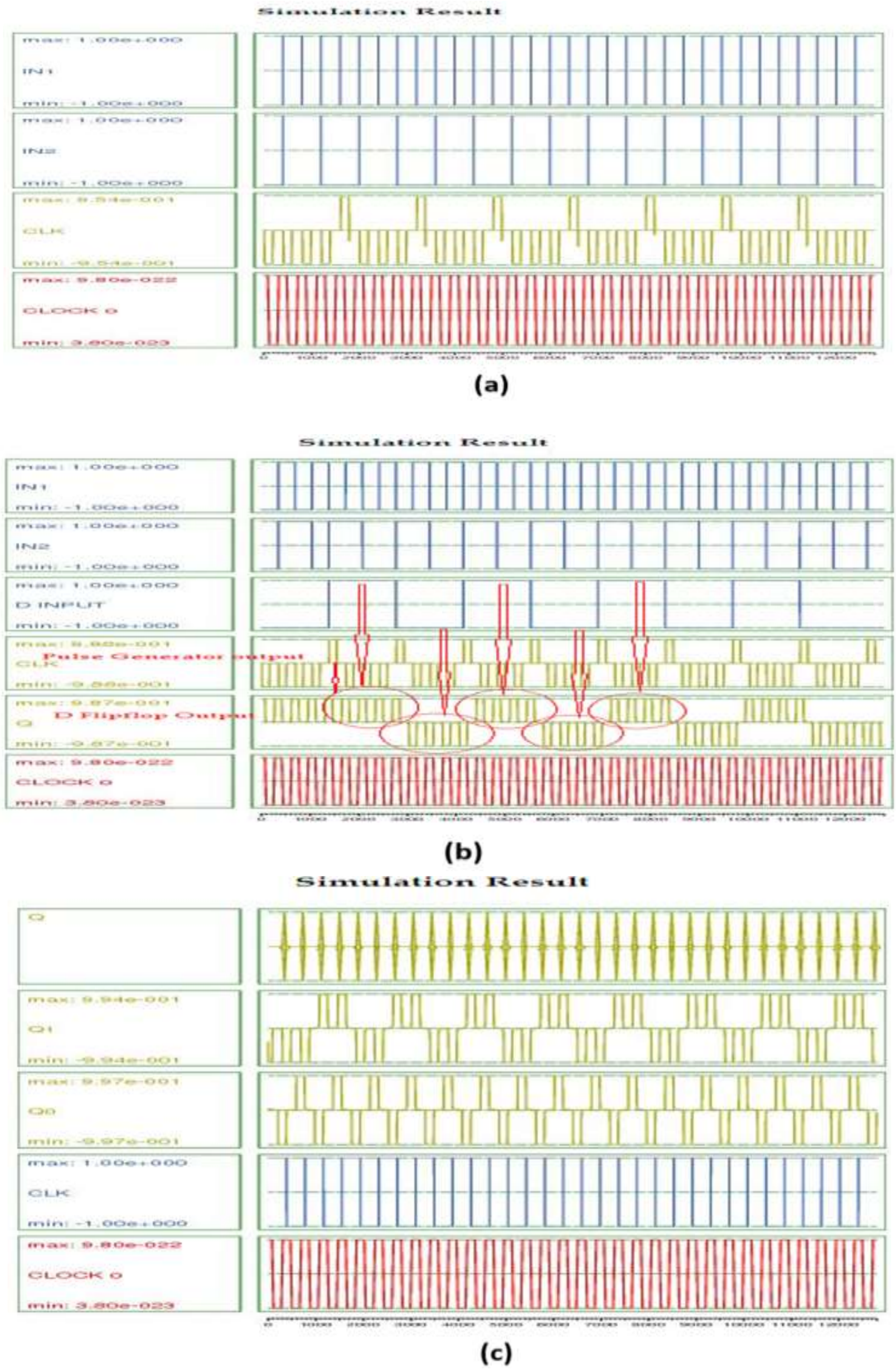
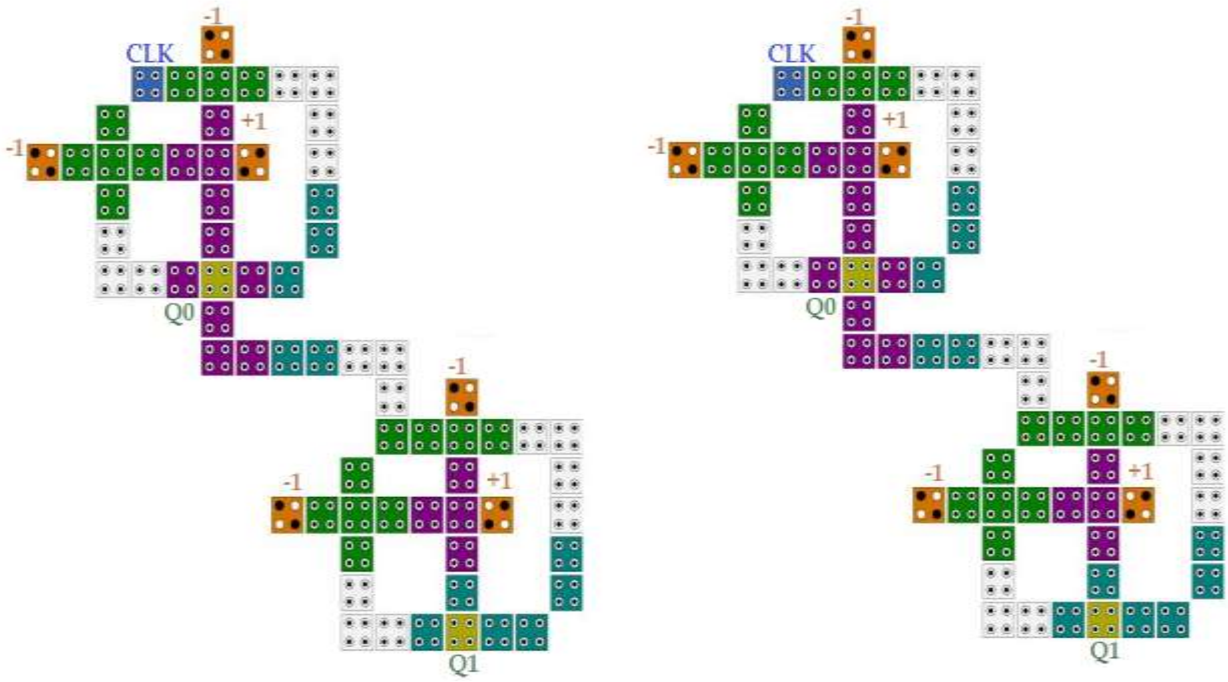


Figure 10. *Simulation outputs for the suggested designs (a)Pulse Generator (b)D type Flipflop (c) Divide by 2 bit counter.*



(a) (b)

Figure 11. *Proposed QCA Layout for Asynchronous Counter (a) 2 bit (b) n bit.*

Table 2. *Comparison table with existing designs.*

Existing in	**No of Cells**	**Area (in µm^2)**	**Latency (in 10^{-12}s)**	**Average Energy dissipation (in eV)**	**Circuit Simulation Time (in Seconds)**
[9]	65	0.07	1.7	2.5e-003	56
[11]	48	0.04	1.5	1.3e-003	39
[13]	33	0.02	1.2	1.7e-003	27
[21]	29	0.02	0.7	1.7e-003	22
[23]	40	0.01	0.5	1.3e-003	30
[31]	25	0.01	0.25	1.4e-003	22
Suggested D type Flip flop	**21**	**0.03**	**0.01**	**6.8e-004**	**18**

Table 3. *Comparison table of QCA Counter with existing work.*

Presented in	**Crossover**	**Cell Count**	**Area (in µm^2)**	**Latency (in 10^{-12}s)**
[19]	No	615	1.0	3
[21]	Yes	422	0.45	1.5
[24]	Yes	285	0.31	1.5
[31]	No	236	0.32	2.0
[32]	No	190	0.20	2.0
Proposed Counter	**Yes**	**110**	**0.28**	**0.5**

It is evident from the simulation results above that the power of the suggested work is lower than that of the current work. The QCA Designer and QCA Designer-E tools, which are described in Tables 2 and 3, were used to conduct this study.

The suggested design has reduced complexity and less power dissipation, based on observations made using different simulation results. Because of its reduced latency and power consumption, the suggested QCA D-FF may be utilized with the development of digital systems.

4. Result and Discussion

In this section the results presented with cell count, area, latency, power dissipation and simulation time for the proposed designs of D type flip-flop and counter. For findings of performance matrices by using QCA Designer tool and to calculate the energy power dissipation can be done by QCA Designer E tool. Every clock cycle with a gain of zero is used to represent this clock sequence. Variable D represents the input waveform with the different binary bit values. In order to send the output waveform, which is represented by the variable Q, the logic first initializes the clock (CLK) as a bit value of 1. Although the waveform changes, the output stays the same. Figures 10(a) and 10(b) show the simulated waveform of the D flip-flop and the stimulated waveform for the pulse generator. Energy levels for the outputs reached the maximum values like ±9.97e-001.In table 2 comparison made with the existing and proposed designs of D type flip-flop with various performance matrices. Table 3 shows the comparison of performance matrices for counter design with existing designs. Figure 10 shows the output waveform, which shows the estimated polarization rate of the two-bit counter, which varies from ±9.94e-001.It is investigated that the accuracy level rises and the suggested QCA D-FF has a greater polarization rate. States like 0(00) to 4(11) are represented by the system's rectangle box. The effectiveness of the suggested QCA implementation is demonstrated by the simulation results.

The simulation research compares the QCA structures' complexity to that of the current designs. Chart 1.Comparision chat existing and suggested D type FF. Similar works were done and reported in the literature [33-39].

5. Conclusion

The suggested work makes a first attempt to create a revolutionary robust Quantum-Dot Cellular Automata (QCA) architecture using an n-bit asynchronous counter and D-Flip Flop (D-FF). The power and implementation complexity that can be shown using the QCA Designer-E tool determine how efficient the designing factor. Quantum-Dot Cellular Automata (QCA) cell design, coverage area, circuit delay factor, and power consideration are some of the metrics that are used in the implemented technology. It is evident from Tables 2 and 3 that the suggested approach, Quantum-Dot Cellular Automata with D-Flip Flop (QCA D-FF), is more efficient than the current design strategy. Since they span a large portion of the circuit, counters are likewise regarded as a key component in the design process. As a consequence, the simulation results of the implemented work shown that it has improved polarization factor with decreasing delay factor, reduced cell usage, and lowest area coverage. Because the suggested approach reduces power consumption and improves performance analysis, it is mostly used in the building of high-speed digital systems.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
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- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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