International Journal of Computational and Experimental Science and ENgineering (IJCESEN)

Vol. 11-No.1 (2025) pp. 306-312
http://www.ijcesen.com

ISSN: 2149-9144

Research Article

Design and Analysis of Novel Full Adder using ECRAAL

S. Nagaraj[1], G. M. Sreerama Reddy[2], S. Aruna Mastani[3]

[1]Research Scholar Department of ECE JNTUA Anantapuramu, AP
* **Corresponding Author Email:** nagarajsubramanyam@gmail.com - **ORCID:** 0000-0002-2190-3706

[2]Prof and Head Department of ECE CBIT Kolar, KA
Email: gmsreeramareddy@gmail.com - **ORCID:** 0000-0001-5872-1941

[3]Asistant Professor Department of ECE JNTUA Anantapuramu, AP
Email: aruna_mastani@yahoo.com - **ORCID:** 0000-0002-9410-5596

Article Info:

DOI: 10.22399/ijcesen.848
Received : 30 November 2024
Accepted : 31 December 2024

Keywords :

Half Adder,
Full Adder,
Adiabatic Logic,
Asy- chronous Adiabatic Logic,
ECRL,
digital circuits.

Abstract:

In VLSI (Very Large Scale Integration) design, adders are digital circuits that perform arithmetic operations, specifically addition, on binary numbers. They are used in many applications, including microprocessors, digital signal processors, and memory systems. An adder is composed of logic gates that take two binary numbers as inputs and produce a binary sum as output. In this paper we have designed and analysed A novel Full Adder circuit by using asychronous adiabatic Logic. ECRAAL means Efficient Charge Recovery Asychronous Adiabatic Logic which combines the ECRL and AAL. ECRAAL is used for implementing Full Adder circuit. The designed ECRAAL Full Adder circuit is compared with the existing ECRL adiabatic Logic in terms of speed, area and power. The Full Adder IS implemented by using TANNER Tools for 250nm Technology. The Novel Full adder has shown improvement in performance. It has decreased 14.71% average power and 50.49% maximum power as compared to ECRL.

1. Introduction

In VLSI (Very Large Scale Integration) design, adders are digital circuits that perform arithmetic operations, specifically addition, on binary numbers. They are used in many applications, including microprocessors, digital signal processors, and memory systems.

An adder is composed of logic gates that take two binary numbers as inputs and produce a binary sum as output. The simplest adder is a half-adder, which adds two single binary digits, but can only produce a sum of 0 or 1. A full-adder, on the other hand, can add three binary digits (two inputs and a carry from a previous addition) and produce a sum of 0, 1, or 2. However, since binary numbers only use 0 and 1, a full-adder must include additional logic to handle the carry, which is the value carried over from one addition to the next [1-15].

They consist of ripple carry adders, carry look ahead adders, carry select adders, carry skip adders. They have different characteristics and trade offs on performance, area, power consumption [1]. One example is simple but requires many stages to add large numbers with ripple carry adders, but they have a slow propagation delay thus not suitable for high frequency applications. Carry-lookahead adders, however, have a smaller number of stages in which to add large numbers, but they require more complex circuitry and consume more power [2]. Different characteristics and trade-offs in terms of performance, area, and power consumption [5]. For example, ripple-carry adders are simple and easy to design, but they have a slow propagation delay and require many stages to add large numbers. Carry-lookahead adders, on the other hand, can add large numbers with fewer stages, but they require more complex circuitry and consume more power [10].

Adders are an important building block in VLSI design and the performance and efficiency of these adders are important components in digital systems performance.

2. Half Adder

Half adder circuit adds the two input bits and give sum and carry out put bits. It is a basic adder circuit. Half Adder block diagram is shown in the Figure 1. There are A and B inputs and Sum and Carry

outputs. If any one of the input is 1 and both inputs are 1 then the sum is 0 and carry is 1. If both inputs are 1, sum is 1, and carry is 0. If both inputs are 0 then sum and carry are both 0. The half adder truth table is displayed in the Table 1. Figure 2 shows the Half Adder circuit diagram implementation using one xor gate and and gate. Table 2 is full adder truth table.

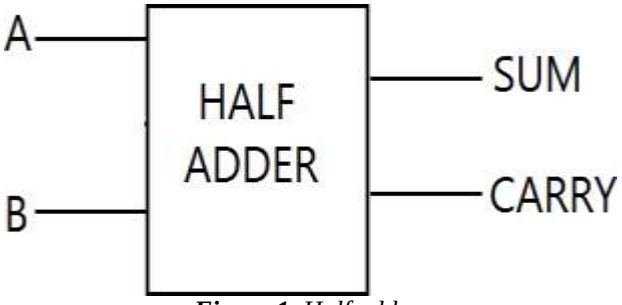

Figure 1. *Half adder.*

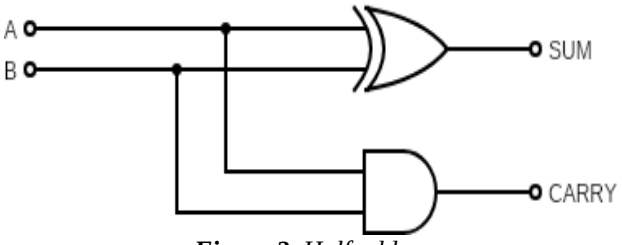

Figure 2*. Half adder.*

3. Full Adder

Full adder has three inputs and two outputs Sum and Carry. The Figure 3 shows Full Adder block diagram Output Sum is zero and carry is zero when all the inputs are zero; Output sum is 1 and carry is zero when any of the input is 1; Output sum is zero and carry is 1 when two of the input is 1; Output sum is zero and carry is 1 when all of the three inputs are 1.

Table 1. *Half adder truth table.*

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

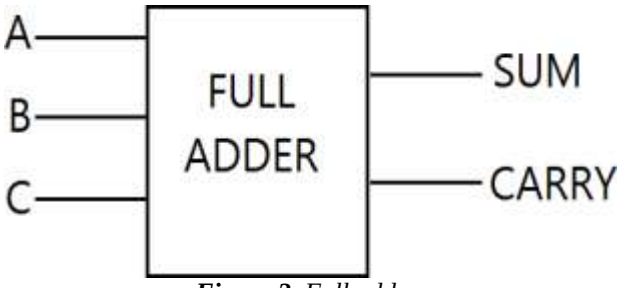

Figure 3. *Full adder.*

Table 2. *Full adder truth table.*

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4. ECRL

Efficient Charge Recovery Logic (ECRL) technique is applied for the design of power management circuits of electronic devices [3,4]. The implementation is used to increase the power management circuitry efficiency and battery life of portable electronic devices [6-9].

Power is recovered by ECRL from charge that otherwise would be lost during the power management process. There is a loss of some of the energy when a power management circuit uses a battery to power a device [11]. This energy loss is exploited by ECRL that captures the energy and stores it in a capacitor for future use.

The charge that was recovered can be used to run the device itself, or stored in the battery to increase the life of the device. It also demonstrates that ECRL can be used to reduce the heat that occurs from the power management circuitry to increase efficiency of the device [12].

Traditionally, ECRL is used with other power management techniques, for example voltage scaling, power gating, adaptive voltage positioning, to build a highly efficient and effective power management system [16]. If ECRL is utilized, it can provide a huge battery life improvement, which in turn is an essential matter for portable electronic devices powered by batteries.

Efficient Charge Recovery Logic (ECRL) offers several advantages in the design of power management circuits for electronic devices:

Improved Efficiency: The power management process causes the charge to be lost and thus ECRL recovers the charge [13,14]. This means that less energy is wasted during the voltage conversion and thus, more energy is available for the use of the device or to prolong the battery life.

Longer Battery Life: ECRL can recover and store the charge lost by the battery in order to extend the life of the battery. That's especially important for small, portable electronic devices where battery life is usually limited.

Reduced Heat Generation: Recovering the energy, and powering the device directly, allows the load on the power management circuitry to be reduced, and

freed from increased heat generated by the circuitry [17-20]. Such improved reliability and longer device lifespan can be anticipated.

Flexible Design: However, ECRL can be coupled with voltage scaling and power gating in order to form a highly efficient and effective power management system [21]. This also enables designers to generate tailored power management solutions to meet the particular requirements of their device.

Cost-Effective: Power management circuits can be made more efficient with ECRL, an inexpensive way to do so. Since this is a method for capturing otherwise lost energy and storing it, this does not require significant additional hardware or components. It becomes a good thing for manufacturers of devices, who want to reduce the energy efficiency involved in product.

ECRL can overall enable large improvements in energy efficiency, device performance and battery life in many power management circuits.

With Efficient Charge Recovery Logic (ECRL) we have several favorable benefits as aspect of power administration design circuits for electronic devices, there are some potential disadvantages to consider:

Complexity: Realizing ECRL may require an extra circuitry, thus complicate the design of power management circuits. But this can make design and testing of the circuits more difficult, lengthening development time and cost.

Increased Circuit Size: Stored energy recovery (ECRL) necessitates the use of a capacitor to store the recovered energy [22]. That can add to the size of the power management circuit, something that needs to be watched when space is limited.

Reduced Voltage Headroom: ECRL can be used to reduce the voltage headroom present in the power management circuit. In some applications, however, this may restrict the voltage range that the circuit can support, excluding certain voltage levels [23].

Limited Efficiency Improvement: For selected energy loss reductions of the voltage conversion during ECRL, the benefits of this approach may be limited. In such cases, ECRL adds substantial complexity, but renders very slight improvement in efficiency.

Capacitor Leakage: The capacitor used in ECRL may experience leakage over time, which can result in energy loss and reduced efficiency. This can be mitigated through the use of high-quality capacitors, but this can increase the cost of the circuit.

Overall, the advantages of ECRL generally outweigh its potential disadvantages, but the decision to use ECRL should be based on the specific needs and requirements of the device being designed.

A functional N block and two cross-coupled PMOS transistors make up the circuit. Due to the circuit's basic partial adiabatic logic design, it has some restrictions. When the power supply exceeds the transistor threshold value, the two cross-coupled PMOS transistors cease to function, causing non-adiabatic losses. The transistor is turned off and the recovery path is cut off when the supply voltage exceeds the transistor's threshold voltage. As a result, recovery is not complete. The coupling effect, which can cause the two outputs to conflict, is another drawback of ECRL. The Figure 4 shows Full Adder block diagram using ECRL. Figure 5 ECRL nand gate and figure 6 ECRL exor gate.

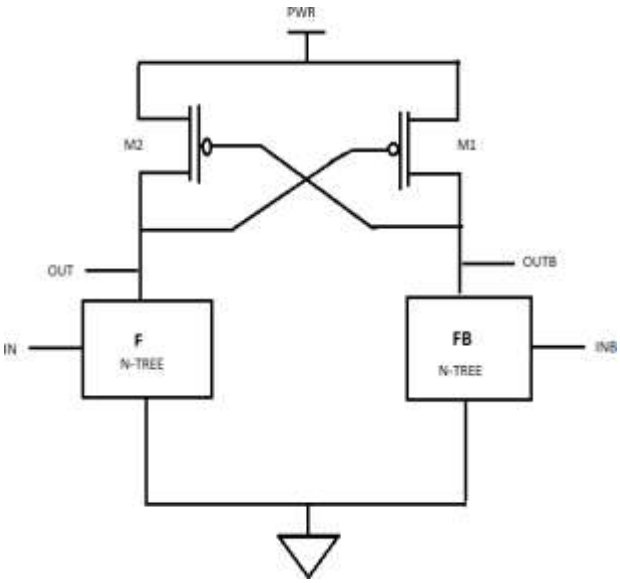

Figure 4. *ECRL.*

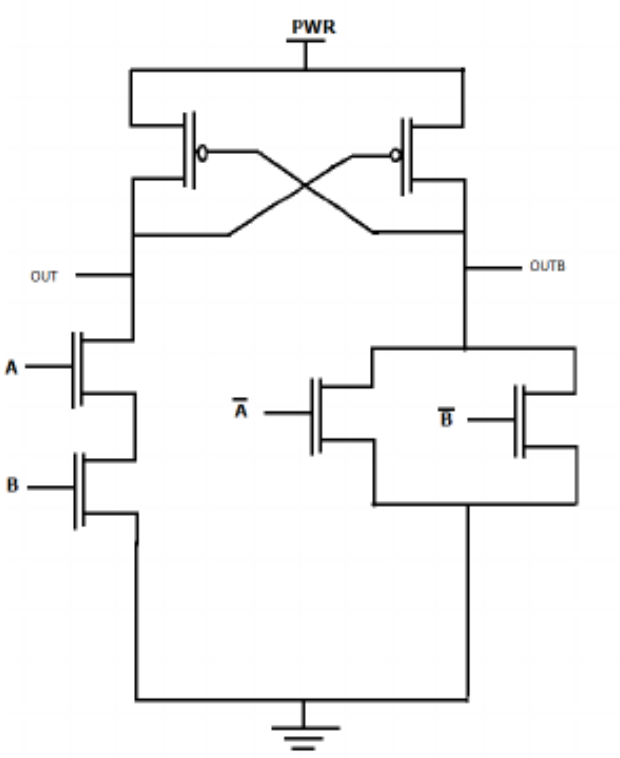

Figure 5. *ECRL nand gate.*

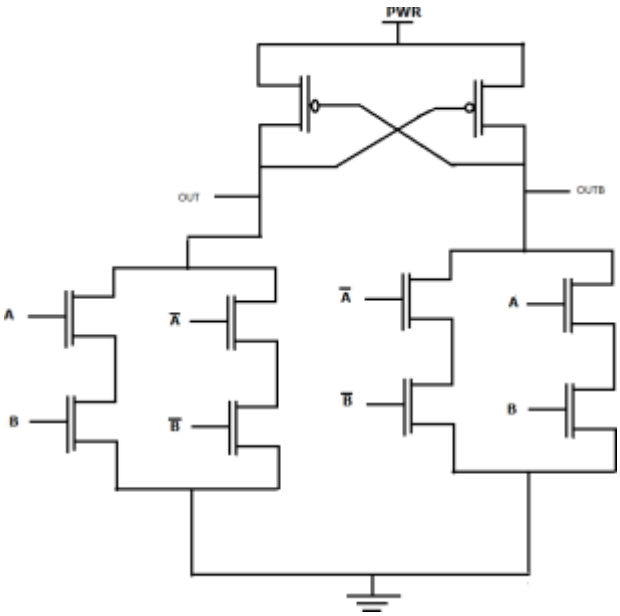

Figure 6. *ECRL exor gate*

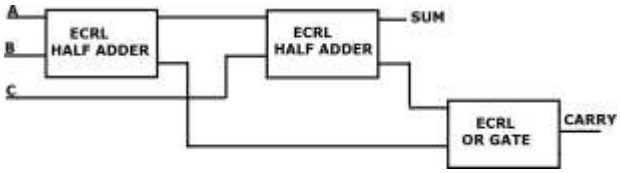

Figure 7. *ECRL full adder.*

5. ECRAAL

ECRAAL means Efficient Charge Recovery Asychronous Adiabatic Logic which combines the ECRL and AAL. Efficient Charge Recovery Asynchronous Adiabatic Logic (ECRAAL) is a logic design technique that aims to reduce the power consumption of digital circuits by using adiabatic principles. Adiabatic circuits are designed to minimize energy consumption by storing and reusing the energy that is normally lost as heat in traditional circuits.

To recycle the dissipation energy during the switching of the digital circuit, ECRAAL uses a charge recovery circuit. The charge recovery circuit is made up of a capacitor and a switch to recover stored and release energy in a controllable manner. Since the energy is usually dissipated as heat, during the charging phase of the capacitor the energy is stored in the capacitor. When the capacitor is discharged, the stored energy is used to power a part of the circuit that follows the capacitor.

In ECRAAL, In traditional synchronous circuits, a clock signal can be a major source of power consumption, ECRAAL uses asynchronous design to get rid of the need of clock signal. Since in asynchronous design, the various parts of the circuit work in separate fashion with the timing being decided after the previous operation is complete or not, it is more prone to errors as and when a signal travels from one place to another. Therefore there is no requirement for clock signal that can give a huge power consumption reducing [24].

ECRAAL is a strong for low power digital circuit design and cutting power consumption by up to 90% when compared to conventional synchronous circuits [25]. Nevertheless, it is still an active area of research and work has to be done to improve its performance as well as resolve its limitations.

However, ECRAAL has several advantages over traditional asynchronous digital circuit design. Some of these advantages include:

Lower power consumption: Evidently, ECRAAL can lower power consumption of traditional synchronous circuits dramatically. With ECRAAL, power consumption can be reduced up to 90%, by using adiabatic principles to recover and reuse energy lost as heat.

Higher energy efficiency: By recycling energy normally lost as heat, ECRAAL can achieve higher energy efficiency than the conventional synchronous circuits. ECRAAL doesn't use a clock signal, and a clock signal can be a significant power drain in traditional synchronous circuits.t design. Some of these advantages include:

Lower power consumption: ECRAAL can significantly reduce power consumption compared to traditional synchronous circuits. By using adiabatic principles to recover and reuse energy that is normally lost as heat, ECRAAL can reduce power consumption by up to 90%. Higher energy efficiency: ECRAAL can achieve higher energy efficiency than traditional synchronous circuits by recycling energy that would otherwise be wasted as heat. Asynchronous design: ECRAAL does not rely on a clock signal, which can be a significant source of power consumption in traditional synchronous circuits. This asynchronous design means that various parts of the circuit will be able to operate independently, decreasing power consumption and providing more flexible and efficient design possibilities. Reduced electromagnetic interference (EMI): Traditional synchronous circuits can significantly suffer from EMC, but ECRAAL can reduce EMI to a great extent. ECRAAL reduces the rapid change in current and voltage through the use of asynchronous design following adiabatic principles so as to reduce EMI.

Improved reliability: Process variations and noise become less detrimental to the reliability of digital circuits and are better addressed with ECRAAL. The ECRAAL uses the adiabatic charge recovery technique to compensate for supply voltage and temperature variations and to enhance the robustness and reliability of the circuit. Overall we find that ECRAAL is a promising technique for low power digital circuit design with several advantages over

traditional synchronous circuits. While it remains still an active area of research, its performance needs further work to be optimized and overcome its limitations.

ECRAAL has some potential disadvantages and limitations which should be considered when designing digital circuits. Some of these include:

Complexity: ECRAAL circuits, especially large scale designs, are more complex than traditional synchronous circuits. However, use of adiabatic principles or asynchronous design can sometimes necessitate additional circuitry and design considerations that potentially increase design time and effort. Limited clock frequency: Like standard synchronous systems, ECRAAL circuits are limited to a low frequency clock. The reason for this is that the ECRAAL adiabatic charge recovery circuit has a minimum amount of time in which to charge and discharge the energy storage elements, limiting the maximum clock frequency of the circuit. Limited noise immunity: Since ECRAAL circuits can be more susceptible to noise than traditional synchronous circuits, their mask filters are based on additional ideas to make them robust in the presence of noise. Use of ECRAAL's asynchronous design and charge recovery technique may increase sensitivity to noise and other external factors that affect the circuit timing and operation. Reduced signal speed: The signal speed of ECRAAL circuits can be slower than that of traditional synchronous circuits. However, if the ECRAAL design had implemented the asynchronous design, it would have latched on through the completion of the previous operation to decide the timing of the next operation, introducing more delay in that circuit. Implementation challenges: Implementation of ECRAAL is generally considered more complicated than implementations of traditional synchronous circuits. ECRAAL will be more, although additional circuitry and design considerations are required for ECRAAL circuit is designed, fabricated, and tested. Overall, ECRAAL is a good technique for low power digital circuit design, however the technique is not perfect and must be considered in circuit design. When designing a circuit for a given application, careful trade offs between power consumption, performance, and circuit level complexity should be considered when selecting a circuit design technique.

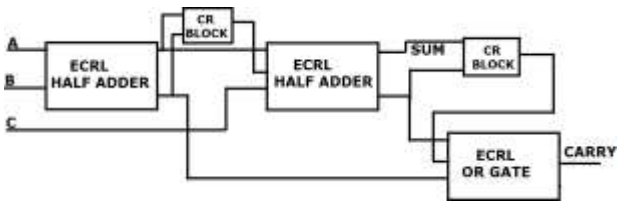

Figure 8. *ECRAAL full adder.*

6. Results

The Figure 7 shows the input and output simulated wave- forms of ECRL Full Adder. The Figure 8 shows the input and output simulated waveforms of ECRAAL Full Adder. Figure 9 is ECRL full adder simulated waveforms and figure 10 ECRAAL full adder simulated waveforms. Figure 11 shows no of transistors in ECRL and ECRAAL and figure 12 shows delay in ECRL and ECRAAL. Figure 13 shows power in ECRL and ECRAAL and figure 14 is power delay product in ECRL and ECRAAL.

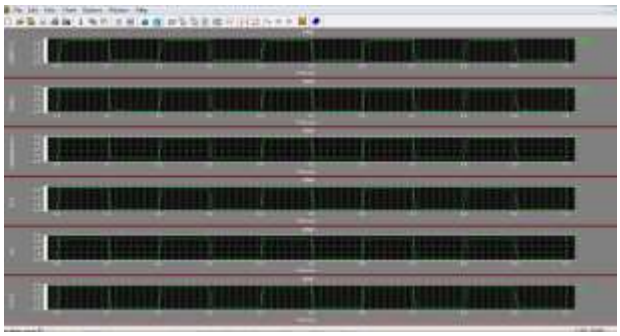

Figure 9. *ECRL full adder simulated waveforms.*

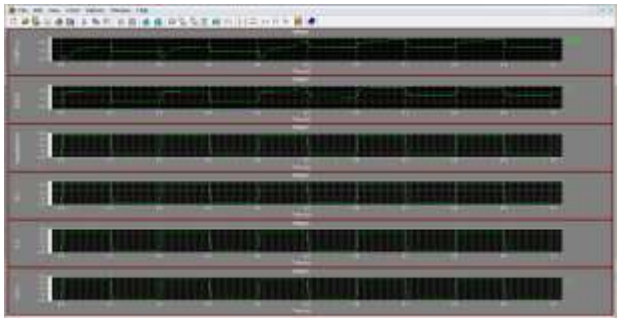

Figure 10. *ECRAAL full adder simulated waveforms.*

7. Conclusion

Thus it can be seen that the praposed ECRAAL Logic has decreaced 14.71 % average power and 50.49 % maximum power as compared to ECRL. The disadvantage is that there is increase of 2.7 % in size of the circuit and 2.68 % increase in delay of ECRAAL as compared to ECRL. But there is 12.42 % decrease of power delay product in ECRAAL as compared to ECRL.Hence we can conclude that ECRAAL is better than ECRL for low power requirements since logic with less power delay product is recommended for low power applications. While table 3 is full adder, table 4 is powers delay product.

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.

Table 3. *Full adder.*

Sno	Logic	No of Tran-sis-tors	Delay (Ps)	Average Power	Max Power	Min Power
1	ECRL	74	511.97	0.265mW	0.406mW	0.25pW
2	ECRAAL	76	525.73	0.226mW	0.201mW	0.25pW

Table 4. *Powers delay product.*

Sno	Logic	Delay (pS)	Power(mW)	Power Delay Product (pS * mW)
1	ECRL	511.97	0.265	135.67205
2	ECRAAL	525.73	0.226	118.81498

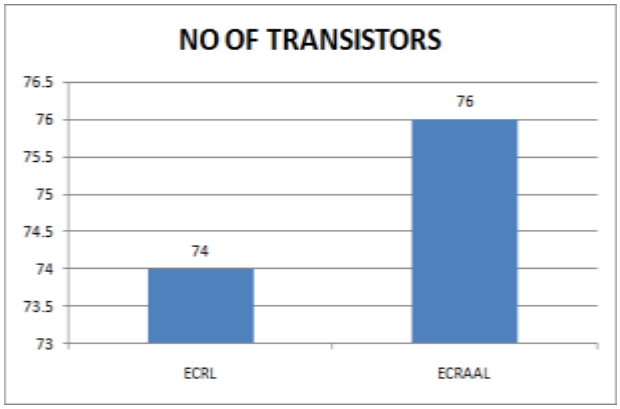

Figure 11. *No of transistors in ECRL and ECRAAL.*

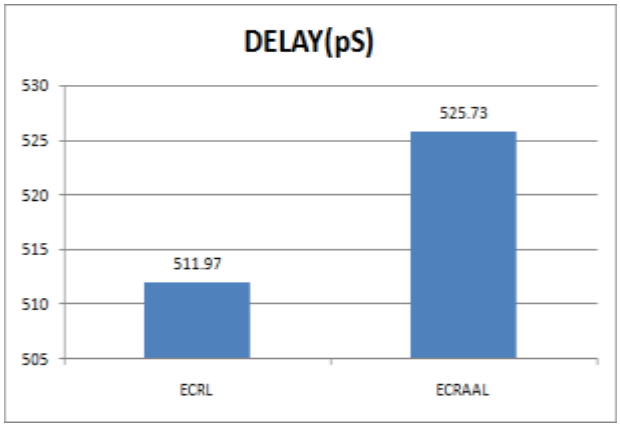

Figure 12. *Delay in ECRL and ECRAAL.*

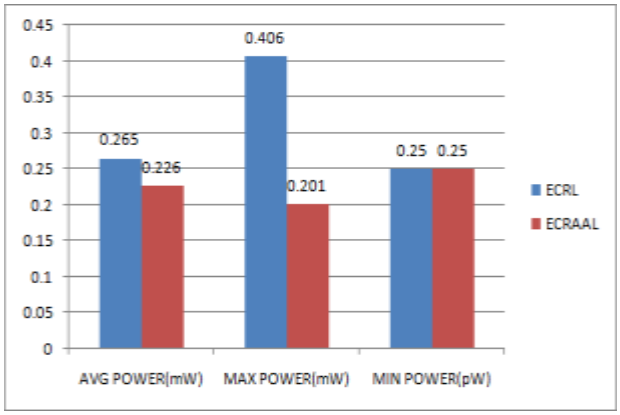

Figure 13. *Power in ECRL and ECRAAL.*

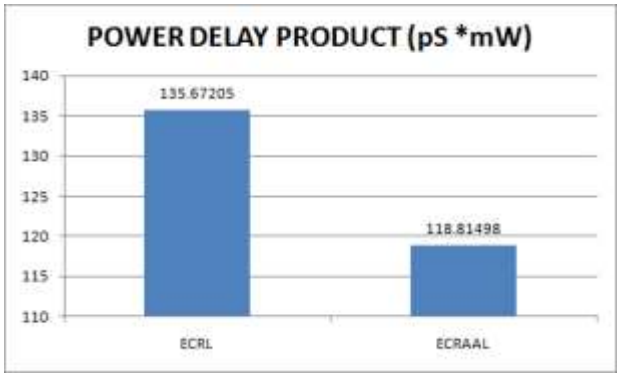

Figure 14. *Power delay product in ECRL and ECRAAL.*

- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
- **Acknowledgement:** The authors declare that they have nobody or no-company to acknowledge.
- **Author contributions:** The authors declare that they have equal right on this paper.
- **Funding information:** The authors declare that there is no funding to be acknowledged.
- **Data availability statement:** The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

References

[1] Morell, W., & Srivastava, A. (2019). Novel, low-power ECRL-CMOS interface circuit. *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*. 25–28. https://doi.org/10.1109/mwscas.2019.8885081.

[2] Kumar, P. V., et al. (2019). Low power ECRL based adiabatic logic for power recycler. *International Journal of Advance Research and Innovative Ideas in Education*. 5(1);1213–1218.

[3] Malhotra, N., et al. (2019). Design of low power ECRL based power gated 4:2 compressor. *2019 6th International Conference on Signal Processing and Integrated Networks (SPIN)*. 891–895. https://doi.org/10.1109/spin.2019.8711712.

[4] Indumathi. (2018). Design and implementation of efficient low power positive feedback adiabatic logic.

[5] Enokido, T., Aikebaier, A., & Takizawa, M. (2011). Computation and Transmission Rate Based Algorithm for Reducing the Total Power Consumption. Journal of Wireless Mobile Networks, Ubiquitous Computing, and Dependable Applications, 2(2), 1-18.

[6] Nagaraj, S., Reddy, G. M. S., & Mastani, S. A. (2017). Analysis of different adders using CMOS, CPL, and DPL logic. *2017 14th IEEE India Council*

International Conference (INDICON). https://doi.org/10.1109/indicon.2017.8487636.

[7] Krishna, B. V., Chakradhar, B., Nagaraj, S., & Prem, P. K. A. (2020). Analysis of Vedic multiplier for conventional CMOS, complementary pass transistor logic (CPL), & double pass transistor logic (DPL) logics. *PalArch's Journal of Archaeology of Egypt/Egyptology*. 17(7);5649–5656.

[8] Agarwal, S., & Sharma, M. (2013). Semi adiabatic ECRL and PFAL full adder. *Computer Science & Information Technology (CS & IT)*. 175–184. DOI : 10.5121/csit.2013.3418.

[9] Moon, Y., & Jeong, D.-K. (1996). An efficient charge recovery logic circuit. *IEEE Journal of Solid-State Circuits*. 31(4);514–522. doi: 10.1109/4.499727.

[10] Jiménez-Carrión, M., Flores-Fernandez, G. A., & Jiménez-Panta, A. B. (2023). Efficient Transit Network Design, Frequency Adjustment, and Fleet Calculation Using Genetic Algorithms. Journal of Internet Services and Information Security, 13(4), 26-49. https://doi.org/10.58346/JISIS.2023.I4.003

[11] Yu, T.-C., Chiu, C.-T., & Kuo, C.-L. (2010). A 1.6 Gb/s charge recovery logic for low-power and high-speed applications. *IEEE Journal of Solid-State Circuits*. 45(12);2631–2640.

[12] Wang, X., Zheng, Y., & Xu, R. (2014). An energy efficient 10 Gb/s charge recovery logic with high linearity and low power consumption. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 22(12);2535–2544.

[13] Kang, D.-S., Lee, S.-J., & Lee, S.-G. (2016). Design of high-speed and low-power charge recovery logic for serial links. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 63(6);547–551.

[14] Sridhar, S., & Kang, S. M. (2002). Design and analysis of a high efficiency charge recovery logic circuit. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 10(6);847–851.

[15] Ebrahim Pakniyat,Seyyed Reza Talebiyan,Milad Jalalian Abbasi Morad and Farnaz Loghmani. (2015). Design of Two New High-Performance Full Adders in Sub-threshold Region for Ultra-Low Power Applications. International Academic Journal of Science and Engineering, 2(2), 73–82.

[16] Kim, H. S., Kim, S. W., & Roy, K. (2006). A high-speed charge recovery logic circuit using dynamic voltage scaling. *IEEE Journal of Solid-State Circuits*, 41(4);904–910.

[17] Babiker, A. H., Al-Qahtani, A. M., & Abd-Alhameed, R. A. (2016). Design of an efficient charge recovery logic for low power high performance applications. *International Journal of Engineering and Technology*. 8(6);2465–2472.

[18] Al-Akhras, S. R., Al-Yamani, A. S., & Al-Harthi, S. H. (2018). Design and implementation of an efficient charge recovery logic for dynamic logic circuits. *International Journal of Electronics and Communications*. 83;366–374.

[19] Li, J., Li, H., & Li, L. (2018). Design of a high-performance charge recovery logic circuit for low-power applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 26(12);2679–2688.

[20] Kwon, J.-K., Jung, W.-S., & Baek, K.-H. (2008). Asynchronous adiabatic logic for low-power digital signal processing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 16(7);867–877.

[21] Shen, J. P. (2002). Adiabatic logic for asynchronous circuits. *Proceedings of the International Symposium on Asynchronous Circuits and Systems (ASYNC)*. 1–10.

[22] Mukherjee, A., & Roy, K. (2010). Asynchronous adiabatic logic design for ultra-low energy applications. *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*. 343–348.

[23] Shen, J. P., & Horowitz, M. A. (2002). Adiabatic asynchronous logic with local clock generation. *Proceedings of the International Conference on Computer Design (ICCD)*. 1–8.

[24] Kinniment, D. J., & Furber, S. B. (2000). A delay-insensitive, adiabatic logic for low power VLSI. *Proceedings of the International Symposium on Asynchronous Circuits and Systems (ASYNC)*. 1–10.

[25] Chahal, S. (2023). A system based on AI and ML enhanced to investigate physiological markers for user forecasting decision-making. *Semiconductor Optoelectronics*. 42(1);1324-1335.